2048-pixel CCD Linear Image Sensor (B/W)

Description

The ILX503A is a reduction type CCD linear sensor designed for facsimile, image scanner and OCR use. This sensor reads B4 size documents at a density of 200 DPI (Dots Per Inch). A built-in timing generator and clock drivers ensure direct drive at 5V logic for easy use.

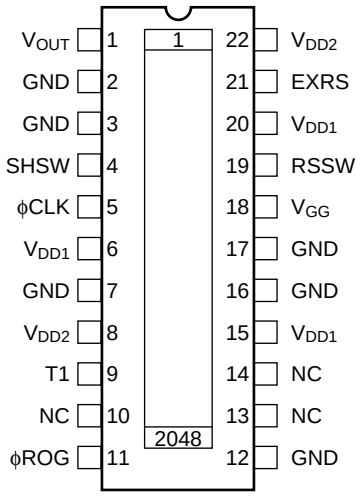
Features

- Number of effective pixels: 2048 pixels
- Pixel size: 14µm x 14µm (14µm pitch)
- Built-in timing generator and clock-drivers
- Ultra low lag
- Maximum clock frequency: 5MHz

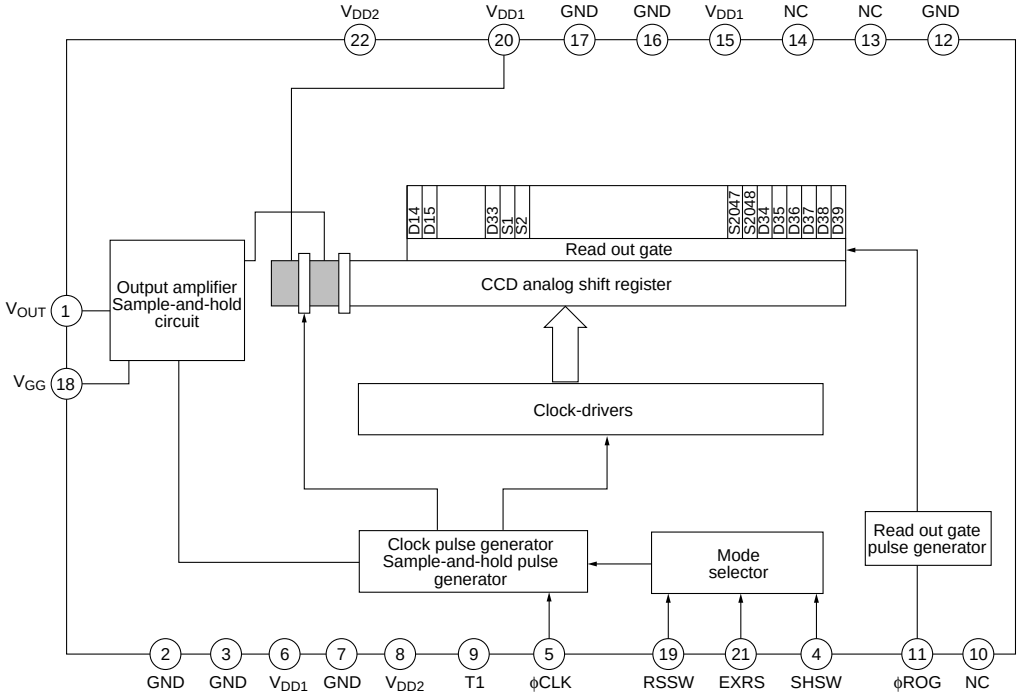
Absolute Maximum Ratings

• Supply voltage	V_{DD1}	11	V
	V_{DD2}	6	V
• Operation temperature		–10 to +55	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	V_{OUT}	Signal output	12	GND	Ground
2	GND	Ground	13	NC	No connect
3	GND	Ground	14	NC	No connect
4	SHSW	Switch (with S/H→GND without S/H→V_{DD2})	15	V_{DD1}	9V power supply
5	φCLK	Clock pulse	16	GND	Ground
6	V_{DD1}	9V power supply	17	GND	Ground
7	GND	Ground	18	V_{GG}	Output circuit gate bias
8	V_{DD2}	5V power supply	19	RSSW	RS pulse external, internal selection (External RS→V_{DD2}, Internal RS→GND)
9	T1	Test pin (V_{DD2})	20	V_{DD1}	9V power supply
10	NC	No connect	21	EXRS	RS input pin during external RS pulse usage
11	φROG	Clock Pulse	22	V_{DD2}	5V power supply

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD1}	8.5	9.0	9.5	V
V_{DD2}	4.75	5.0	5.25	V

NOTES:

Rules for raising and lowering power supply voltage:

To raise power supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V).

To lower voltage, first lower V_{DD2} (5V) and then V_{DD1} (9V).

Mode Description

Mode In Use		Pin Condition		
RS	S/H	4-Pin SHSW	19-Pin RSSW	21-Pin EXRS
Internal	Yes	GND	GND	V_{DD2}
	No	V_{DD2}	GND	V_{DD2}
External	Yes	—	—	—
	No	V_{DD2}	V_{DD2}	φ RS

Input Capacity of Pins

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of φCLK pin	CφCLK	—	10	—	pF
Input capacityof φROG pin	CφROG	—	10	—	pF
Input capacity of EXRS pin	C_{EXRS}	—	10	—	pF

Recommended Input Pulse Voltage

Parameter	Min.	Typ.	Max.	Unit
Input clock high level	4.5	5.0	5.5	V
Input clock low level	0.0	—	0.5	V

Electro-optical Characteristics (Ta = +25°C, V_{DD1} = 9V, V_{DD2} = 5V, Clock frequency: 1MHz, Light source = 3200K, IR cut filter: CM-500S (t = 1.0mm), When Internal RS)

Item	Symbol	Min .	Typ.	Max.	Unit	Remark
Sensitivity 1	R1	22.5	30	37.5	V/(lx • s)	(1)
Sensitivity 2	R2	—	95	—	V/(lx • s)	(2)
Sensitivity 3	R3	—	20	—	V/(lx • s)	(3)
Sensitivity 4	R4	—	500	—	V/(lx • s)	(4)
Sensitivity non-uniformity	PRNU	—	2.0	8.0	%	(5)
Saturation output voltage	V_{SAT}	1.5	1.8	—	V	—
Dark voltage average	V_{DRK}	—	0.3	2.0	mV	(6)
Dark signal non-uniformity	DSNU	—	0.5	3.0	mV	(6)
Image lag	IL	—	0.02	—	%	(7)
Dynamic range	DR	750	6000	—	—	(8)
Saturation exposure	SE	0.040	0.060	—	lx • s	(9)
9V supply current	I_{VDD1}	—	8.0	14.0	mA	—
5V supply current	I_{VDD2}	—	3.0	6.0	mA	—
Total transfer efficiency	TTE	92.0	97.0	—	%	—
Output impedance	Zo	—	600	—	Ω	—
Offset level	Vos	—	4.5	—	V	(10)

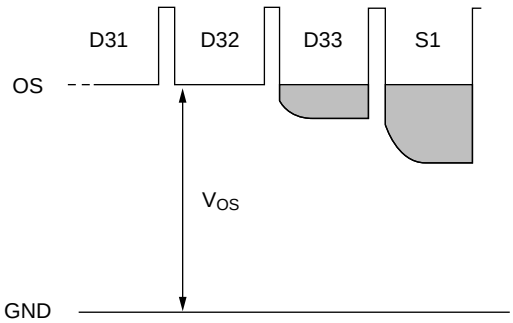
NOTES:

1) For the sensitivity test light is applied with a uniform intensity of illumination.
2) W lamp (2854K)
3) Light source: LED λ = 570nm
4) Light source: LED λ = 660nm
5) PRNU is defined.as indicated below. Ray incidence conditions are the same as for Note 1.

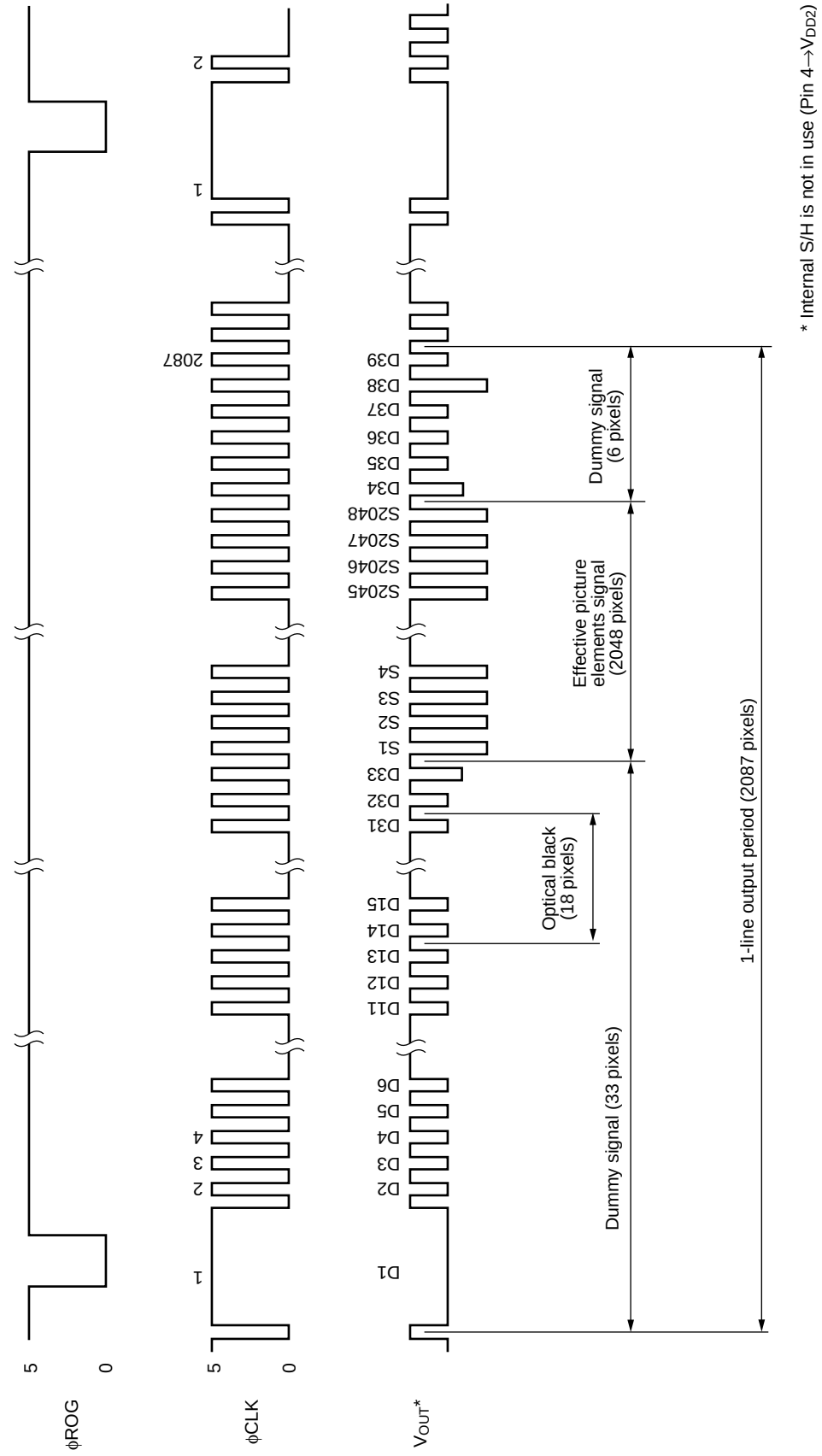
$$PRNU = \frac{(V_{MAX}-V_{MIN})/2}{V_{AVE}} \times 100\ (\%)$$

The maximum output is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

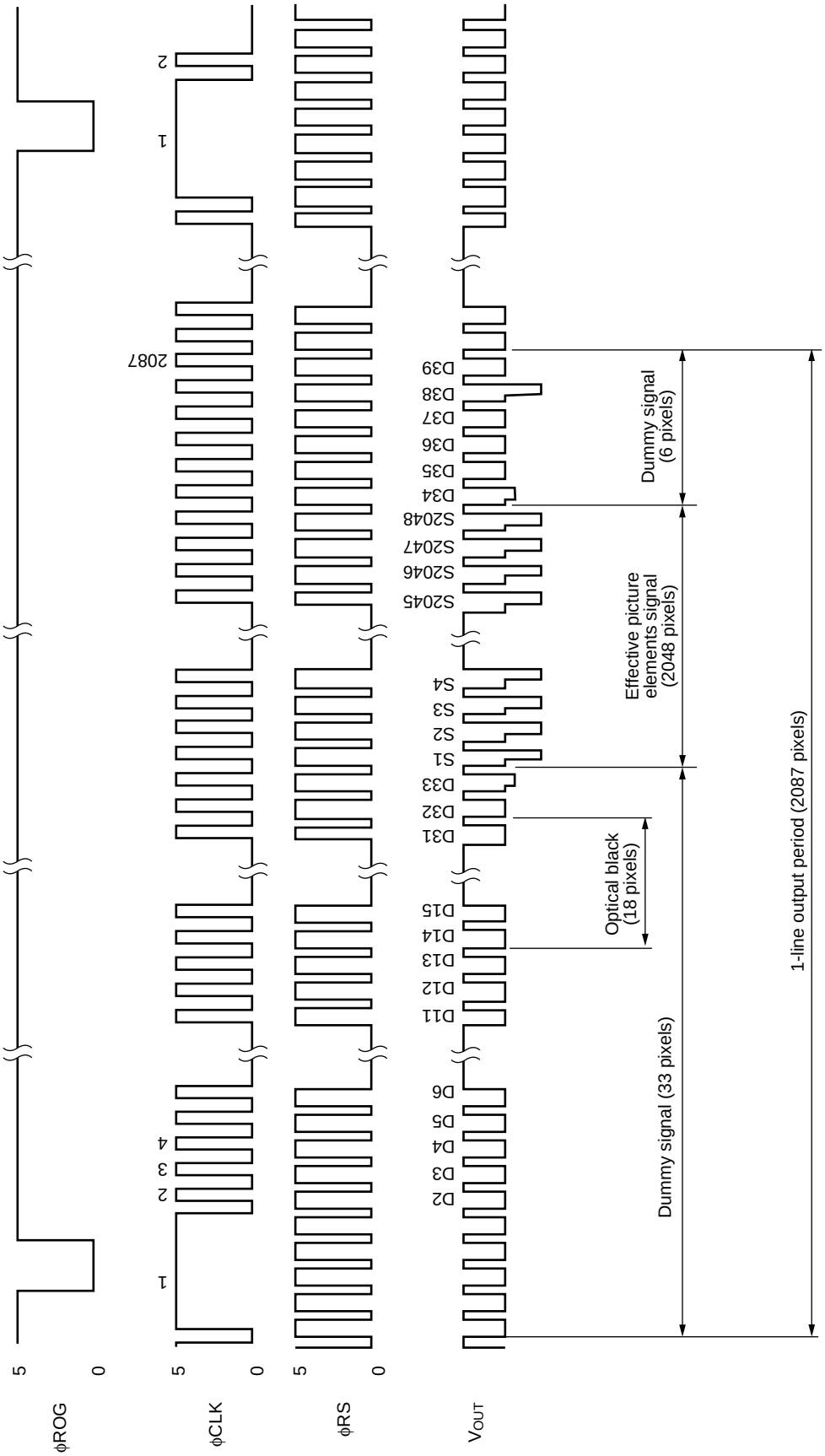
6) Integration time is 10ms.
7) V_{OUT} = 500mV
8) DR = V_{SAT}/V_{DRK}
9) SE = V_{SAT}/R1
10) Vos is defined as indicated below:



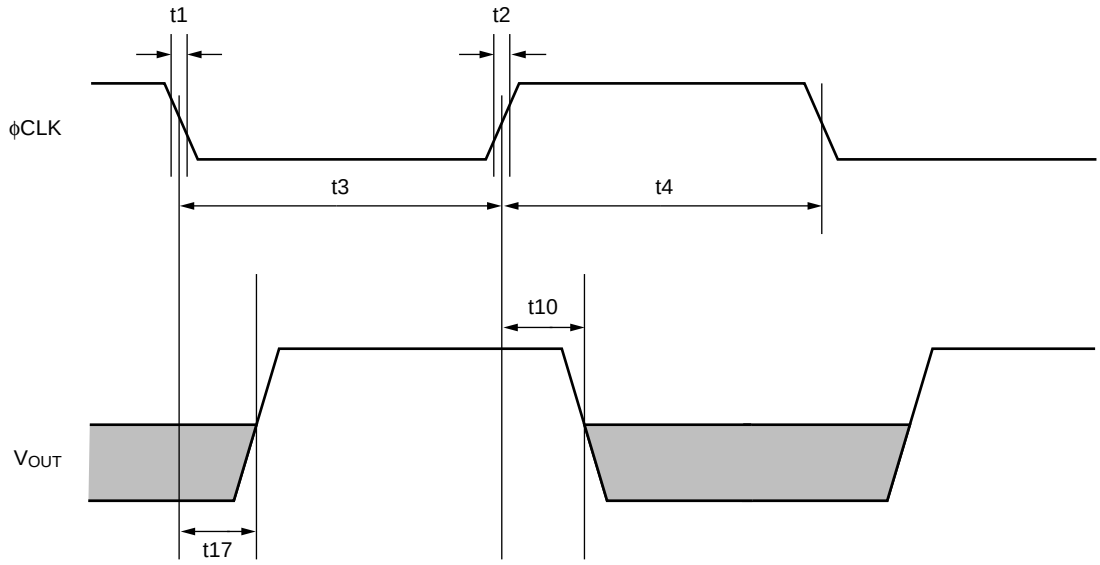
Clock Timing Diagrams (For Internal RS mode)



Clock Timing Diagrams (For External RS mode)



φCLK, VOUT Timing (For Internal RS Mode)

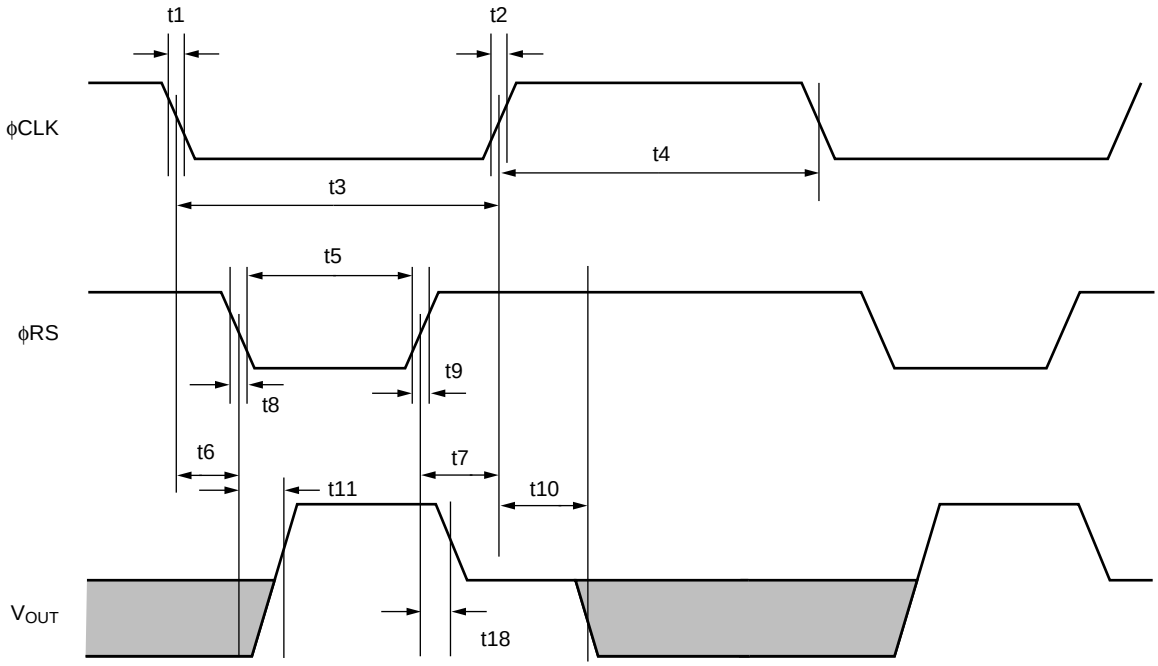


Item	Symbol	Min.	Typ.	Max.	Unit
φCLK pulse rise/fall time	t1, t2	0	10	—	ns
φCLK pulse duty (1)	—	40	50	60	%
φCLK-VOUT 1	t10	50	80	110	ns
φCLK-VOUT 2	t17	30	75	120	ns

NOTE:

1) 100xt3/(t3+t4)

φCLK, φRS, VOUT Timing (For External RS Mode)

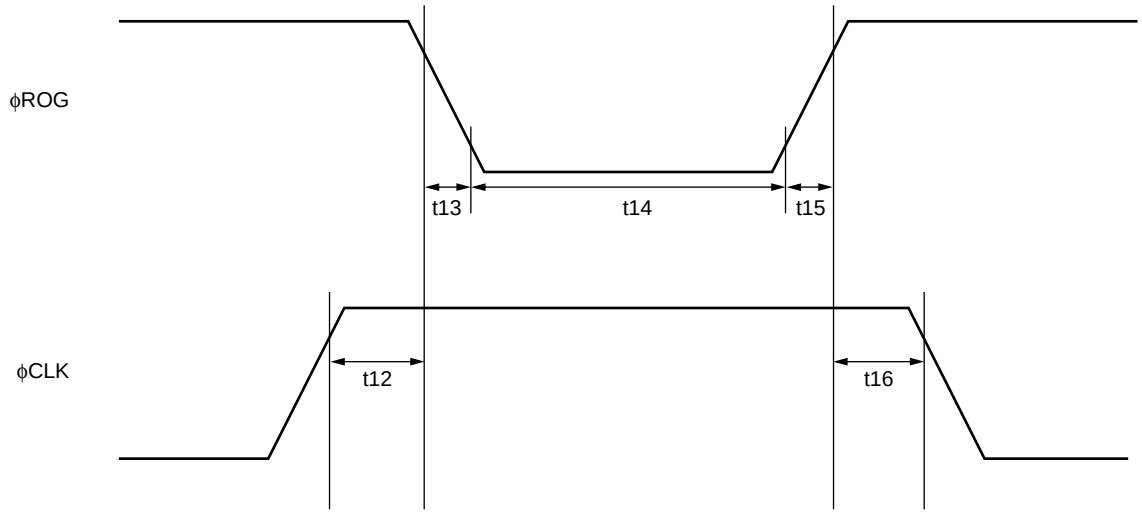


Item	Symbol	Min.	Typ.	Max.	Unit
φCLK, φRS pulse rise/fall time	t1, t2, t8, t9	—	10	50	ns
φCLK pulse duty (1)	—	40	50	60	%
φCLK- φRS pulse timing	t6	0	100	—	ns
φCLK- φRS pulse timing	t7	50	100	—	ns
φRS pulse period	t5	50	100	—	ns
φCLK-V_{OUT}	t10	50	80	110	ns
φRS-VOUT	t11, t18	30	50	70	ns

NOTE:

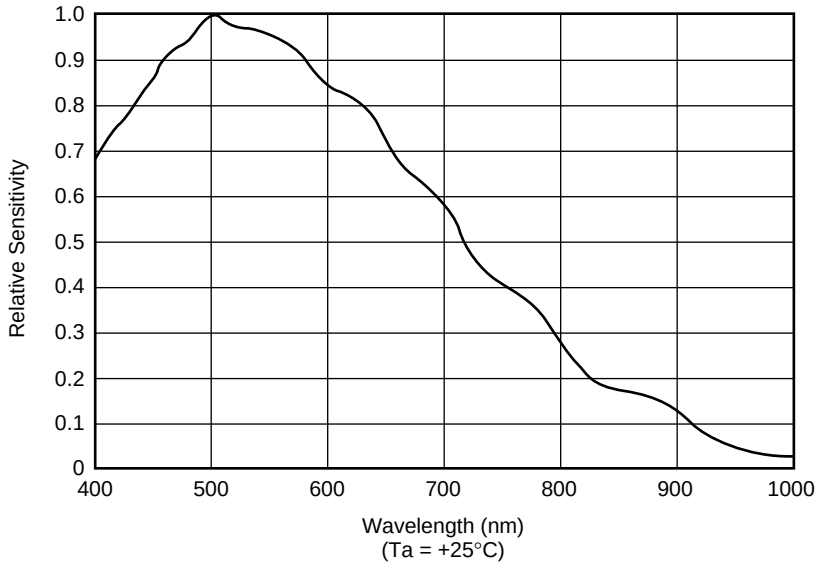
1. 100xt3/(t3+t4)

φROG, φCLK Timing

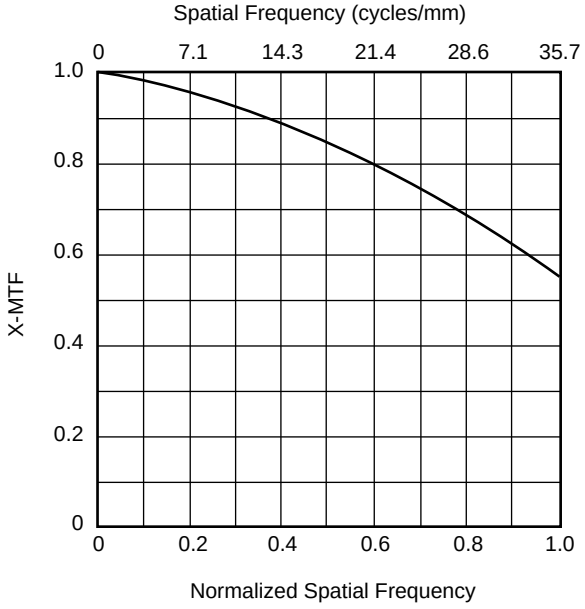


Item	Symbol	Min.	Typ.	Max.	Unit
φROG - φCLK pulse timing	t12, t16	500	1000	—	ns
φROG pulse rise/fall time	t13, t15	0	10	—	ns
φROG pulse period	t14	500	1000	—	ns

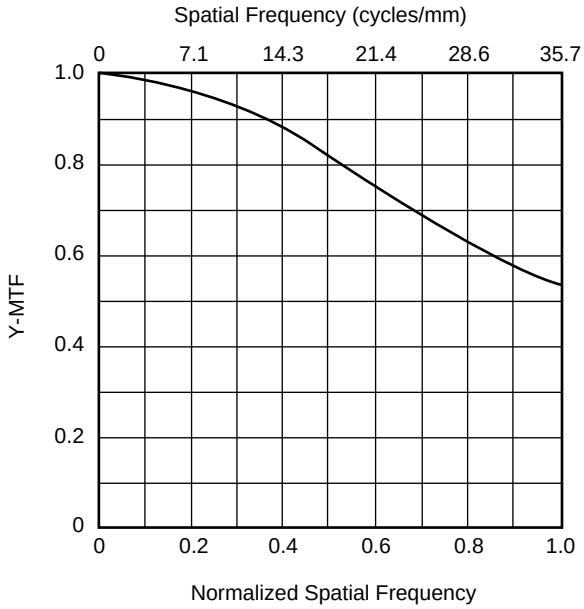
Spectral Sensitivity Characteristics
(Standard Characteristics)



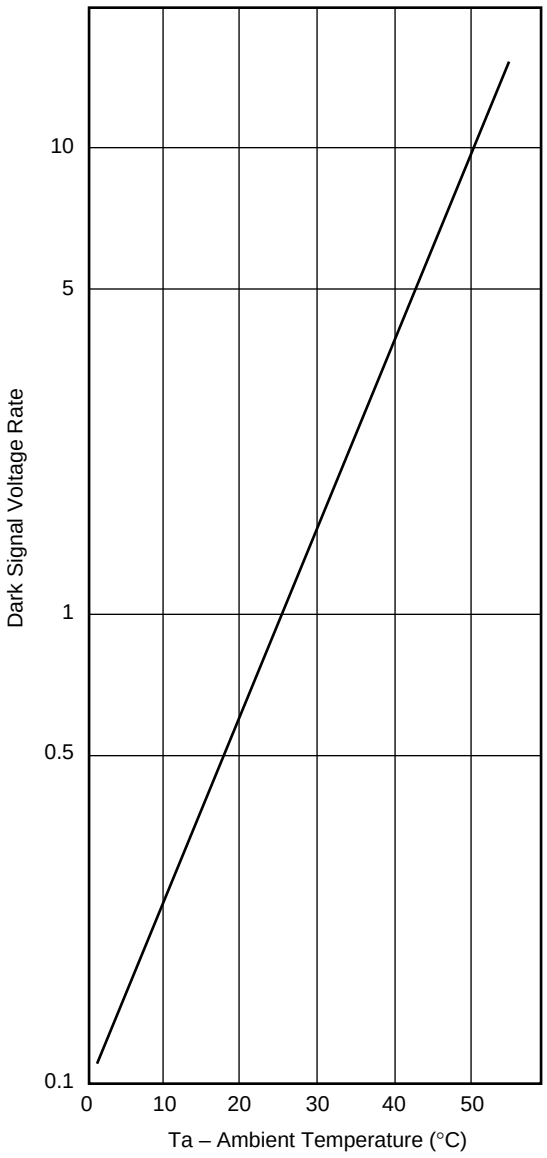
MTF of Main Scanning Direction
(Standard Characteristics)



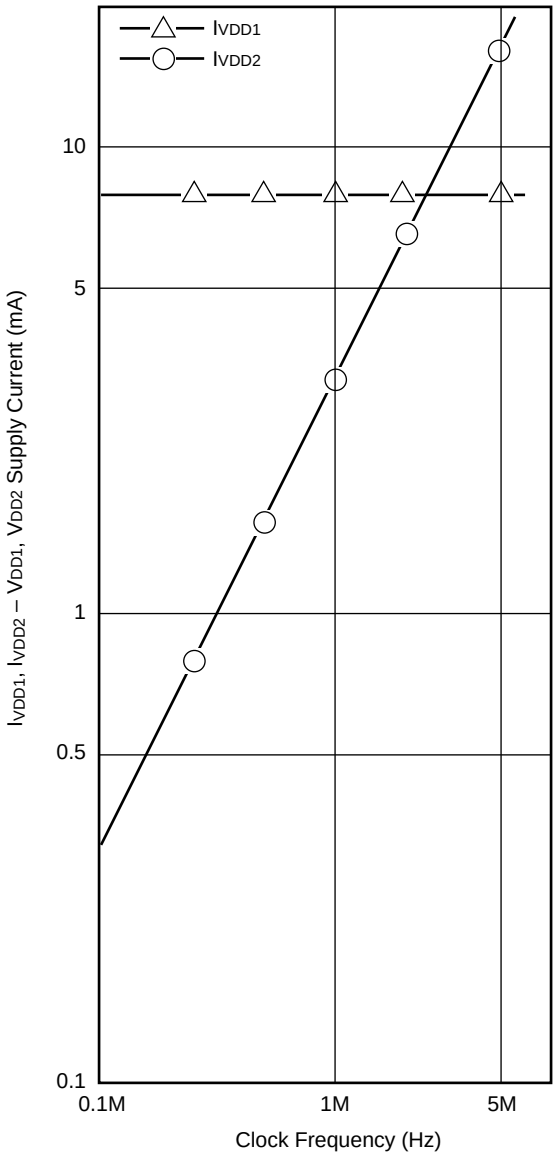
MTF of Sub Scanning Direction
(Standard Characteristics)



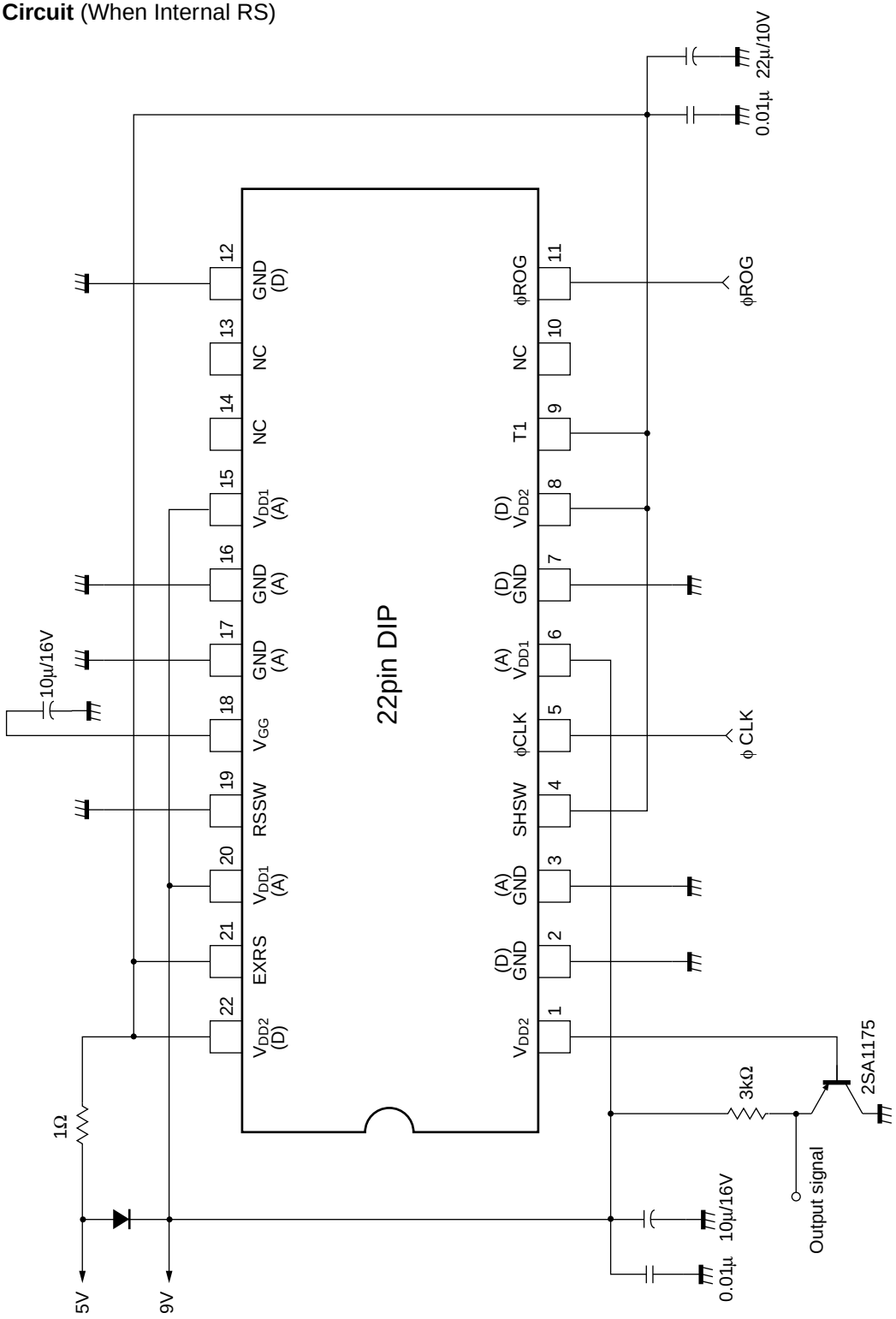
Dark Signal Voltage Rate vs. Ambient Temperature (Typical Characteristics)



V_{DD1}, V_{DD2}, Supply Current vs. Clock Frequency (Typical Characteristics)



Application Circuit (When Internal RS)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infrindgement of third party patents and other rights due to same.

Notes on Handling

1) Static charge prevention

   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures:

   a) Handle with bare hands or use non-chargeable gloves, clothes or material. Also use conductive shoes.

   b) When handling directly, use a grounding band.

   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

   d) Ionized air is recommended for discharge when handling CCD image sensor.

   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Regulation for raising and lowering the power supply voltage:

   When raising the supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V). Similarly, lower V_{DD2} (5V) first and then V_{DDI} (9V).

3) Soldering

   a) Make sure the package temperature does not exceed +80°C .

   b) Solder dipping in a mounting furnace may cause damage or defects to the glass. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

   c) Do not use solder suction equipment to dismount an imaging device. When using an electric desoldering too, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection

   a) Operate in a clean environment.

   b) Do not touch glass plates by hand or have any object come in contact with glass surface. Should dirt stick to a glass surface blow it off with an air blower. (For dirt stuck through static electricity, ionized air is recommended.)

   c) If the glass surface is grease stained, clean with a cotton swab and ethyl alcohol. Be careful not to scratch the glass.

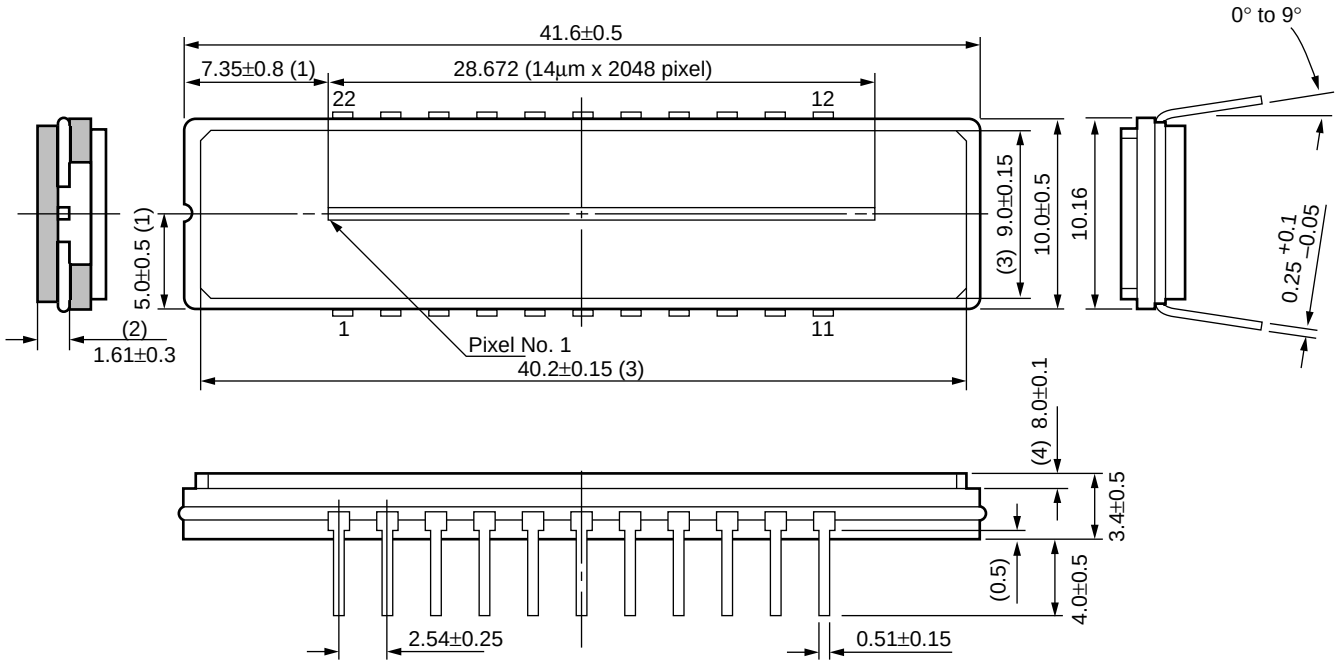
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with a great temperature difference.

5) Exposure to high temperatures or humidity will affect the characteristics. Therefore, avoid storage or usage in such conditions.

6) A CCD image sensor is precise optical equipment that should not be subjected to mechanical shocks.

Package Outline Unit: mm

22 Pin DIP (Cer-DIP) 400mil 3.9g



SONY CODE	LB-1A
EIAJ CODE	WDIP022-G-0400-B
JEDEC CODE	

NOTES:
1) The distance from the package pin side to the first pixel.
2) The distance from the package bottom side to the surface of the sensor.
3) Glass package outline
4) Glass thickness (Index of refraction = 1.5)