

Linear Image Sensor

Product Name

C106

Approval

Notes

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Approved

Checked

Designed

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All specifications of this device are subject to change without notice.

Revision control sheet

Revision No.	Date	Item of change and content	Reason	Approved	Designed

C106 PRODUCT SPECIFICATIONS

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Introduction

1. Features:

- 64 x 1 image sensing elements
- 8 dots per millimeter (dpm) resolution, (200 dpi)
- 125 μm pixel center-to-center spacing
- High sensitivity
- Internal gain
- Single 5 V power supply
- Low power consumption: 10mW maximum
- Single analog video output signal
- On-chip analog video switch

2. Description:

The C106 linear image sensor consists of 64 photo detectors, associated multiplexing switches, shift registers, chip selector logic, odd-even circuitry, and analog video switch. The area of the pixel element is approximately $5400 \mu\text{m}^2$ with 125 μm center to center spacing. Each photo detector is reset more than once during a clock cycle to reduce the image lag. The odd photo detector and the even photo detector are combined into one video output signal. The photo detectors operate in a serial-dump and serial-readout fashion with a series of active shift registers. The device is easily operated with a start pulse (ϕ_{Sp}), a clock pulse (ϕ_{Cp}), and a single 5V power supply.

The chip selector logic is used to activate the output of the individual chips, making them suitable for silicon butting to form a full width linear Contact Image Sensor (CIS) array. These chips can be butted with each other to form a long image sensor module, allowing the length of the module to be extended to A6, A4, B4, A3, ... up to A0 size. Electrically, the start pulse (ϕ_{Sp}) of the second chip is connected to the end of pulse (ϕ_{Ep}) of the first chip, etc. This device can also be used in a wide variety of applications including mark readers, bar code readers, OCR, edge detectors, positioning and optical encoding.

Terminal Description

Terminal Number	Symbol	Name	Description
1	ϕ_{Sp}	Start pulse terminal	To apply a pulse to start signal integration
2	ϕ_{Cp}	Clock pulse terminal	To apply an external clock pulse to chip
3	Vdd	Positive power supply terminal	To connect + 5 V normally
4	Gnd	Ground terminal	To connect to 0 V normally
5	Iout	Video signal output terminal	Send the photo current signal out
6	Gnd	Ground terminal	Connected to pin # 4 inside the chip
7	ϕ_{Ep}	End of pulse terminal	Send a pulse to indicate an end of scan

Table 1. Terminal Description

Functional Block Diagram

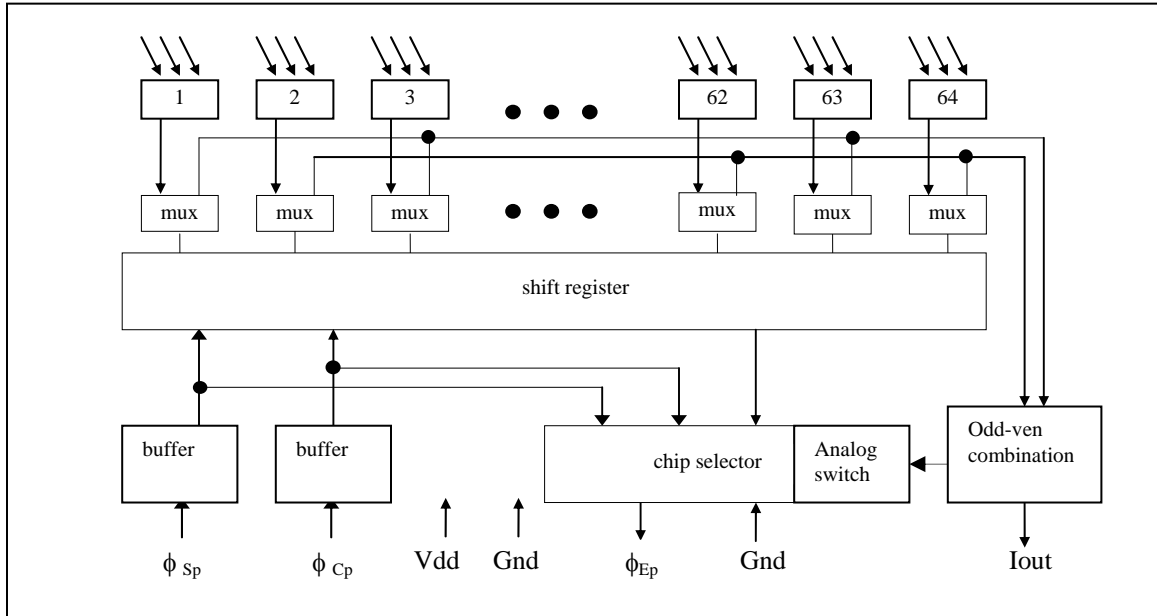


Figure 1. Functional Block Diagram

Bonding Pad Layout Diagram

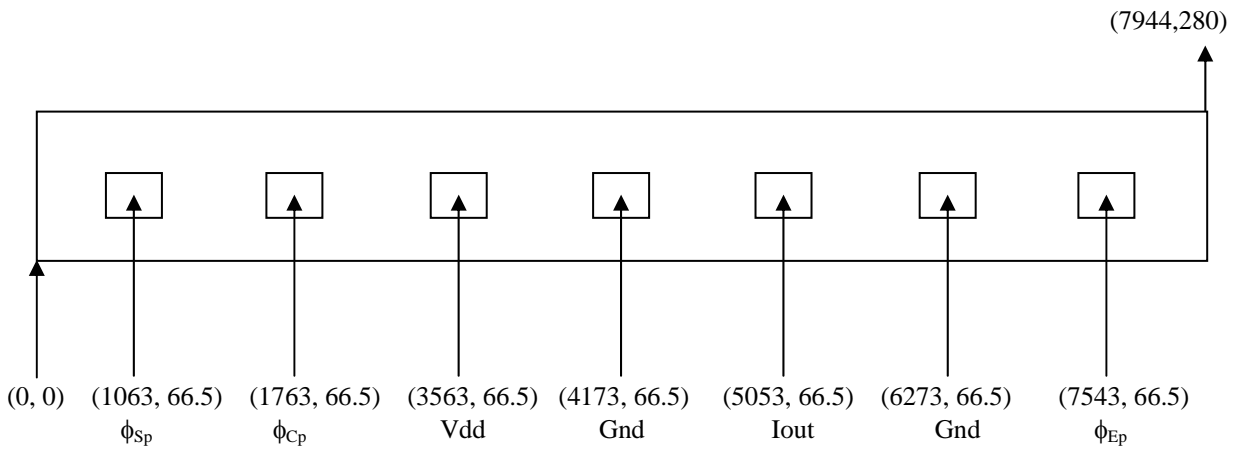


Figure 2. Bonding pad layout diagram

Bonding Pad Description

Pin #	Symbol	Location (x , y) in unit of μm	Description
1	ϕ_{Sp}	(1063, 66.5)	Start pulse
2	ϕ_{Cp}	(1763, 66.5)	Clock pulse
3	Vdd	(3563, 66.5)	Power supply voltage: + 5V
4*	Gnd	(4173, 66.5)	Ground : 0 V
5	Iout	(5053, 66.5)	Current video signal output
6*	Gnd	(6273, 66.5)	Ground: 0 V
7	ϕ_{Ep}	(7543, 66.5)	End of pulse

Table 2. Bonding pad description

Note: Origin: (0 μm , 0 μm) at the lower, left side of the chip.
 Location: (x μm , y μm) is measured at the center of the pad.
 Pad size: (125 μm by 90 μm)
 Chip size: (7944 μm by 280 μm) for the chip.
 (8000 μm by 340 μm), including the scribe lines.
 * Pin # 4 is connected to pin # 6 inside the chip.

Electro-Optical Characteristics

Test conditions:

Measured at $\phi_{\text{Cp}} = 500 \text{ kHz}$, Vdd = 5V, $t_{\text{int}}^{*(1)} = 2 \text{ ms}$, $\lambda^{*(2)} = 565 \text{ nm}$, $C_{\text{ext}}^{*(3)} = 47 \text{ pF}$, Gain^{*(4)} = 2,
 TA^{*(5)} = 25 °C, light intensity = 7.2 LUX.

[See readout circuitry (unless otherwise noted).]

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$V_c^{*(6)}$	Compensated analog output voltage	Light on	400	700	1000	mV
$U_c^{*(7)}$	Compensated nonuniformity	Pixel 2 ~ 63**, within a chip	-10	---	+10	%
$U_{\text{p}_5\text{pix}}^{*(8)}$	5 pixel white level nonuniformity	Every 5 pixels, within a chip	-7.5	---	7.5	%
$U_{\text{cadj}}^{*(9)}$	Compensated adjacent pixel nonuniformity	Within a chip	-7	---	7	%
$C_c^{*(10)}$	Chip-chip compensated nonuniformity	Within a wafer	-13	---	+13	%
$V_d^{*(11)}$	Analog output voltage at dark level	Light off	-200	---	+100	mV
$U_d^{*(12)}$	Dark signal nonuniformity	Within a chip	---	---	100	mV
$C_d^{*(13)}$	Chip-chip dark signal nonuniformity	Within a wafer	---	---	200	mV
I_{dd}	Power supply current		---	---	2	mA

Table 3. Electro-Optical characteristics

Definition:

1. t_{int} is the integration time, which is equal to the interval between two start pulses.
2. λ is the wavelength of the light source.
3. C_{ext} is the off-chip load capacitance for I_{out} .
4. Gain is the gain of an off-chip video operation amplifier.
5. TA is the ambient temperature.
6. $V_c = (V_{cmax} + V_{cmin}) / 2$
 where V_{cmax} is the maximum compensated voltage of the whole array.
 V_{cmin} is the minimum compensated voltage of the whole array.
7. U_c is the pixel-to-pixel compensated photo response nonuniformity within a chip.
 $U_c = [((V_{cmax} - V_{cmin})/2) / V_c] \times 100\%$
8. $U_{p_5pix} = \frac{\text{Max}\{ \text{Max}[V_p(i), V_p(i+1), \dots, V_p(i+4)] - \text{Min}[V_p(i), V_p(i+1), \dots, V_p(i+4)] \}}{\text{Max}[V_p(i), V_p(i+1), \dots, V_p(i+4)] + \text{Min}[V_p(i), V_p(i+1), \dots, V_p(i+4)]}$
 $(i = 1, 2, \dots, 60)$
 where $V_p(i)$ is the video signal output of a pixel # i
 $V_p(i+1)$ is the video signal output of a pixel # $(i+1)$
 \vdots
 \vdots
 $V_p(i+4)$ is the video signal output of a pixel # $(i+4)$
9. $U_{cadj} = \text{Max} [|V_c(i) - V_c(i+1)| / V_c(i)] \times 100\%$, $(i = 2, 3, \dots, 63)$
 where $V_c(i)$ is the compensated video signal output of a pixel # i
 $V_c(i+1)$ is the compensated video signal output of a pixel # $(i+1)$
10. C_c is the chip-to-chip compensated photo response nonuniformity within a wafer
 $C_c = [(V_c - V_{cavg}) / V_{cavg}] \times 100\%$
 where V_{cavg} is the average compensated output signal of all chips within a wafer
11. $V_d = (V_{dmax} + V_{dmin}) / 2$
 where V_{dmax} is the maximum dark voltage of the whole array.
 V_{dmin} is the minimum dark voltage of the whole array.
12. $U_d = V_{dmax} - V_{dmin}$
13. C_d is the chip-to-chip dark voltage nonuniformity within a wafer.
 $C_d = V_d - V_{davg}$
 where V_{davg} is the average dark voltage of all chips within a wafer.

** Pixel # 1 and # 64 measured by U_{p_5pix}

Recommended Operating Conditions

Item	Symbol	Min	Typ.	Max	Unit
Power supply voltage	Vdd	4.5	5	5.5	V
Power supply current	Idd			2	mA
Input voltage	V _i			Vdd	V
High level input voltage	V _{ih}	4		Vdd	V
Low level input voltage	V _{iL}	0		0.8	V
Clock frequency	f	5	500	3000	kHz
Sensor integration time	t _{int}		2.5		ms
Wavelength of light source	λ	400		700	nm
Clock pulse high duty cycle		25	50	75	%
Operating free-air temperature	Ta	0		50	°C

Table 6. Recommended operating Conditions

Absolute Maximum Rating

Power supply voltage, Vdd	-----	7 V
Power supply current, Idd	-----	2 mA
Digital input voltage range, Vih	-----	Vdd
Digital input current range, Iih	-----	- 2 mA to + 2 mA
Operating free-air temperature range, Ta	-----	0 °C ~ 50 °C
Storage temperature range, Tstg	-----	- 25 °C ~ 70 °C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Timing Diagram

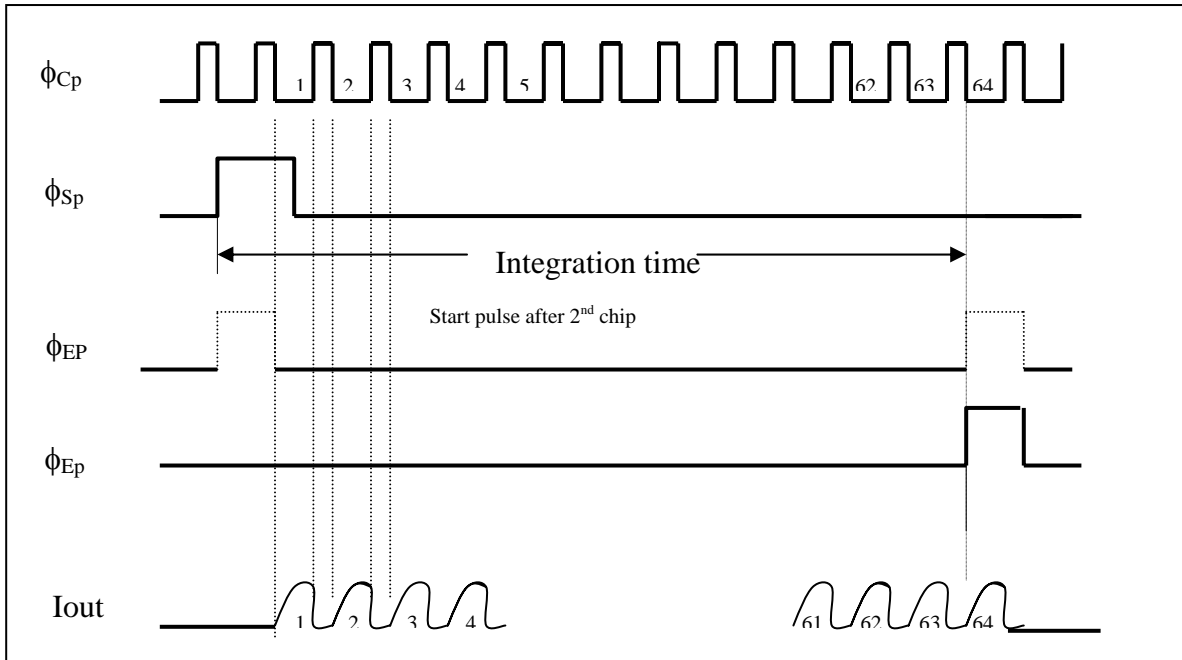


Figure 3. Timing diagram

Readout Circuitry

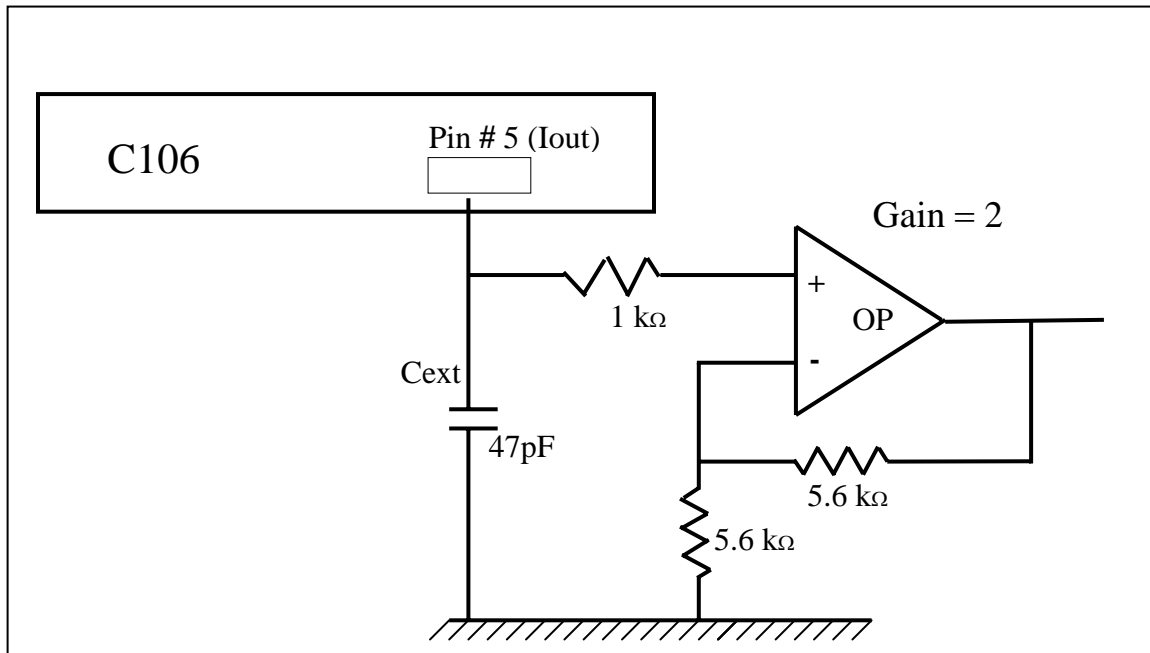


Figure 4. Readout circuitry

Switching Characteristics

Item	Description	Symbol	Min	Typ.	Max	Unit
1	Clock cycle time	t_o		2		μs
2	Clock pulse duty cycle: t_w / t_o			25		%
3	Clock pulse width	t_w		500		ns
4	ϕ_{Sp} setup time	t_{ss}	50			ns
5	ϕ_{Sp} hold time	t_{sh}	50			ns
6	Video digital delay time	t_d		68	800	ns
7	Video signal invalid time	t_i		25		ns
8	Video signal stable time	t_s	36			ns

Table 7. Switching characteristics

Switching Waveforms

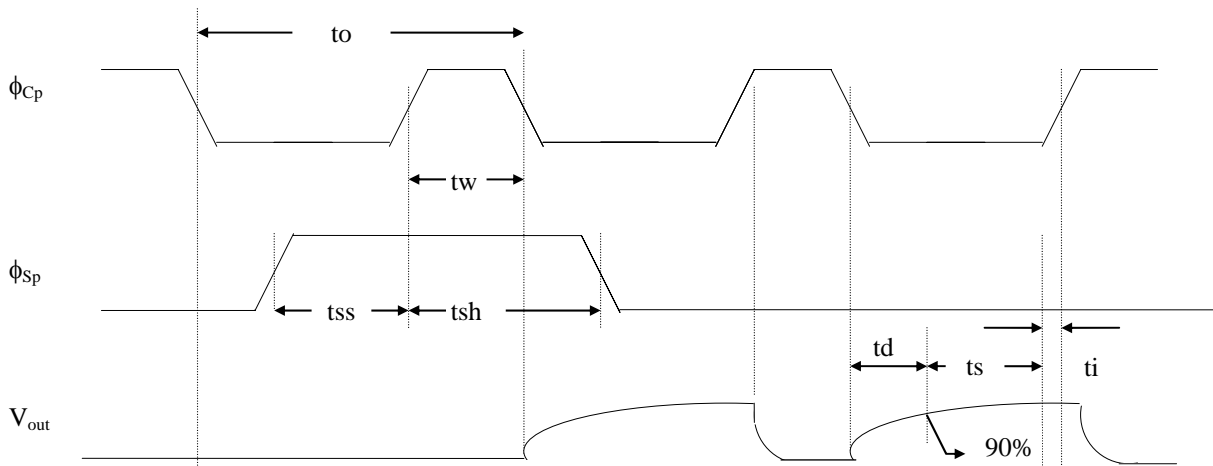


Figure 5. Switching waveforms

QUALITY DOCUMENT

This document applies to the image sensor products of CMOS Sensor Inc., regarding the product applications, product specifications and quality assurance to ensure customer satisfaction.

Quality Specifications

1. Reliability Test Items

No.	Test Item	Test Conditions	Test Time	LTR
1	Biased high temp./ humidity	Ta = 85 °C, RH = 85%, Vabsmax x 0.9	1000 hr.	10%
2	Biased high temperature	Ta = 125 °C, Vabsmax x 0.9	1000 hr.	10%
3	Normal operation	Ta = 25 °C, Vopmax	1000 hr.	10%
4	EDS	C = 200 pF, V = 200 V to Vss, Vdd	1	
5	Latch-up	V = ± 100V, C = 200 pF, V = Vopmax	1	

Note: Vabsmax: Absolute maximum voltage.
Vopmax: Maximum operational voltage.
Test Conditions can be discussed between two parties.

2. Conditions:

If there is any disagreement on any test item described above, both parties should discuss the issues to solve the discrepancies.

Outgoing Inspection

1. Every wafer of the same lot should be processed in the same lot during manufacturing.

2. Inspection Items

2.1. Visual Inspection:

- 1) Lot numbers, wafer numbers.
- 2) Wafer surface color.
- 3) Surface conditions:
 - (a) Contamination
 - (b) Particle
 - (c) Scratch

2.2. Microscope Inspection:

- 1) Instrument: Metallurgical microscope.
- 2) Magnitude: x100 in bright field.
- 3) Criterion: See attached microscope inspection criterion.
- 4) Inspection method: Five points inspection as shown in Figure 1:
 - 1: Center
 - 2: Top
 - 3: Bottom
 - 4: Left with more than 10 mm from the wafer edge.
 - 5: Right with more than 10 mm from the wafer edge

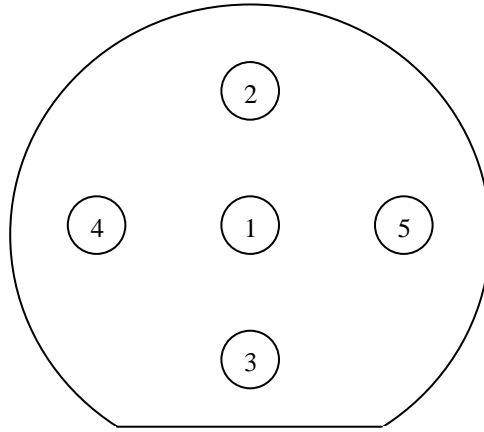


Figure 1. Five points inspection position on a wafer.

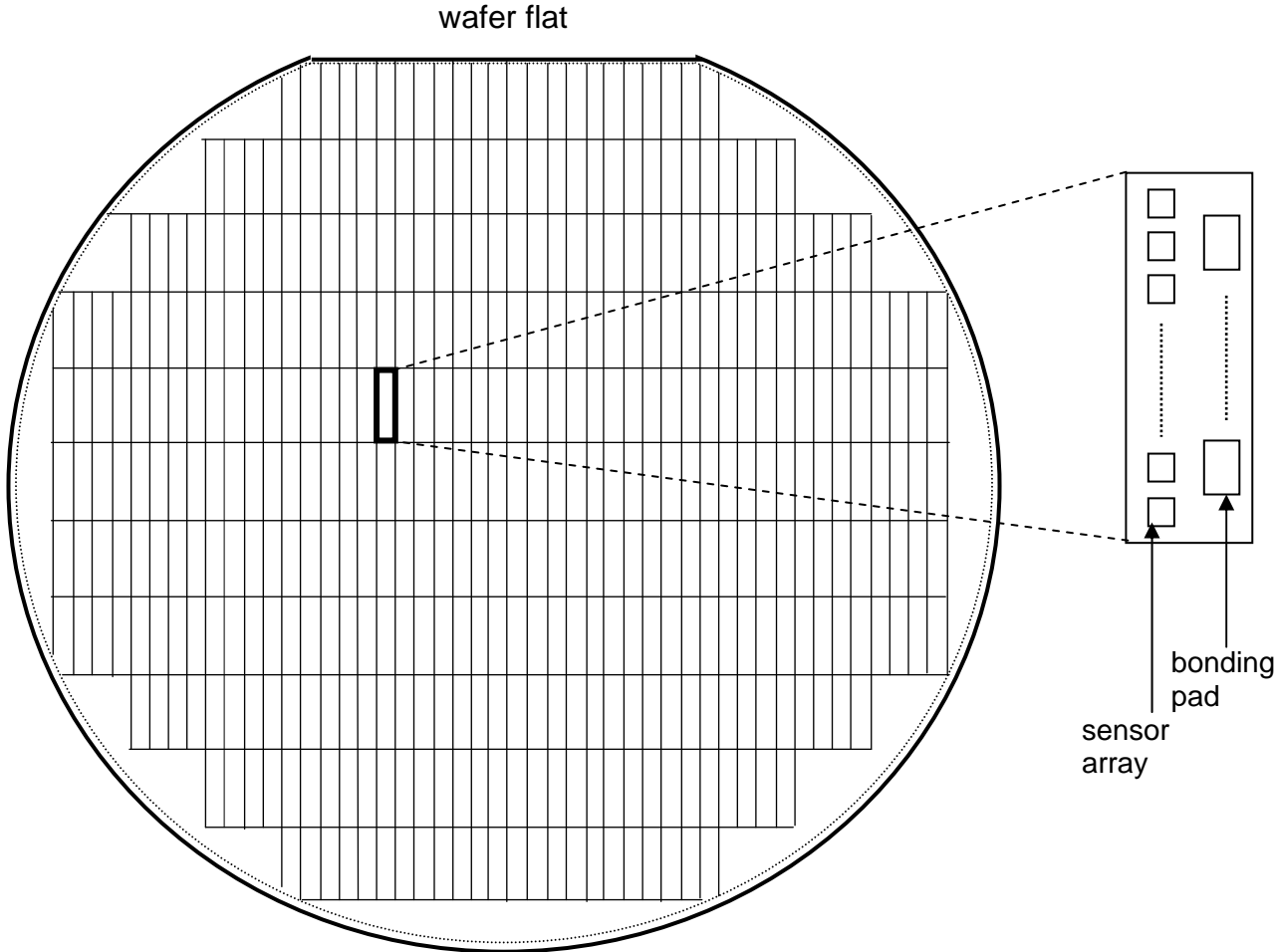
- 5) Sampling method:
 - (a) 100% inspection for the lot with fewer than 5 wafers.
 - (b) 5 wafers plus 20% of the lot size for the lot with more than 5 wafers.
 - 6) Inspection pass criterion:
 - (a) Per wafer: AQL = 0.4%
 - (b) Per lot: AQL = 0.4%
 - 7) Tools during wafer handling:
 - (a) Tweezers or a vacuum van.
 - (b) ESD gloves or finger cots
3. Wafer shipping criterion
 - 3.1. Per wafer: The yield per individual wafer must be greater than 60%.
 - 3.2. Per lot: The average lot yield must be greater than 60%.
 4. Discrepancy resolution
 - 4.1. Any discrepancy should be investigated to determine the cause of this discrepancy and to explore the probable solutions to the issue.
 - 4.2. The returned product will be analyzed to clarify the responsibility. If CMOS bears the responsibility, the deficit will be fully compensated.
 5. Product Modification

Any modification request from either party should be made in writing and may not be carried out without an agreement by both parties.
 6. Product warranty

Product is guaranteed for its performance according to the specs of this document one year from date of receiving the product without any mishandling of the product during the warranty period.
 7. Others

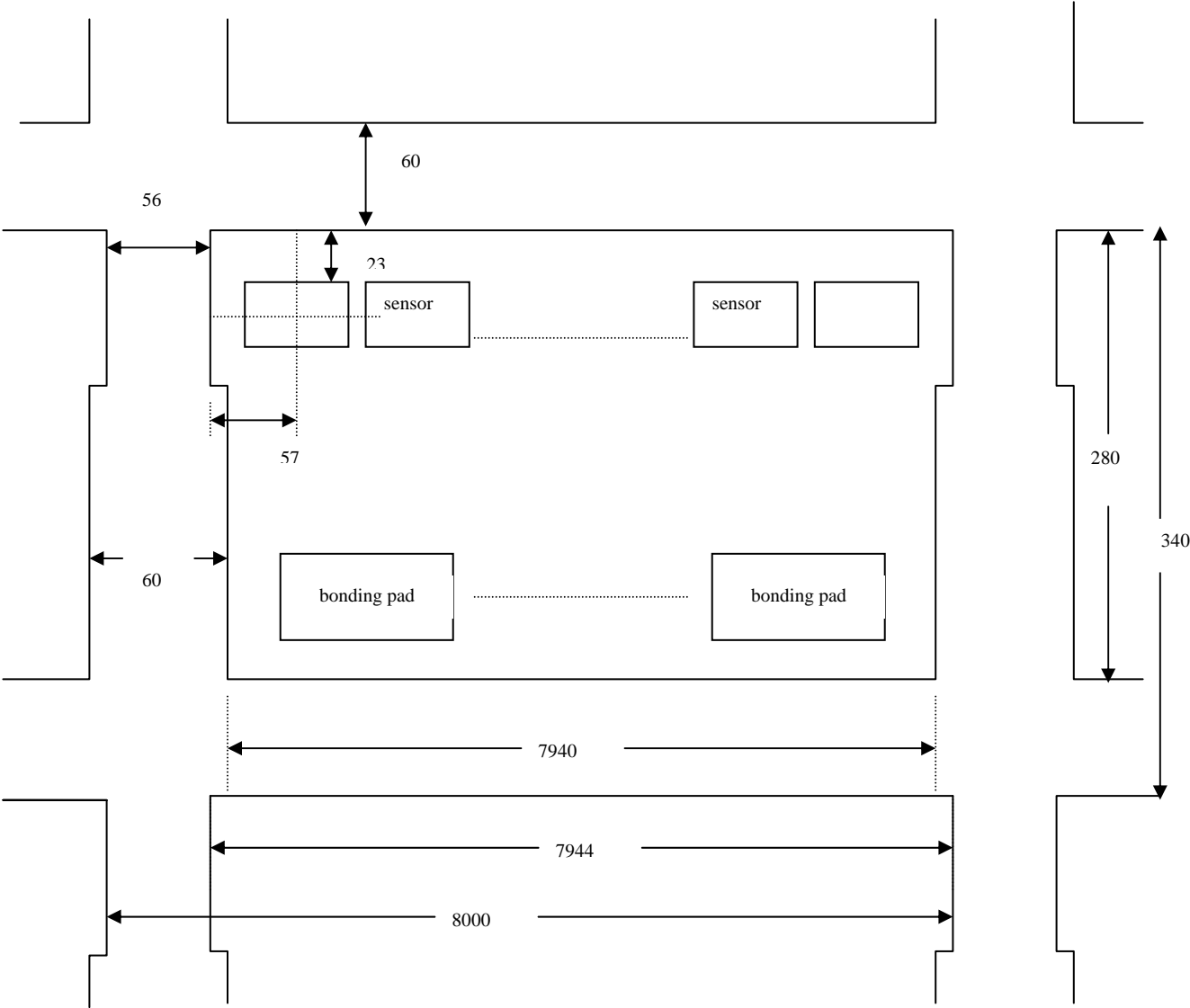
This document can be modified if necessary when both parties agree.

IC Chip Layout on a Wafer



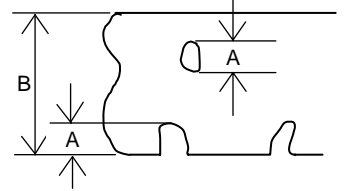
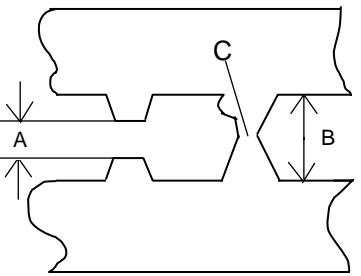
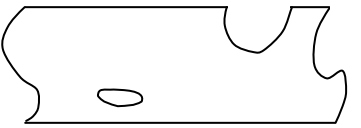
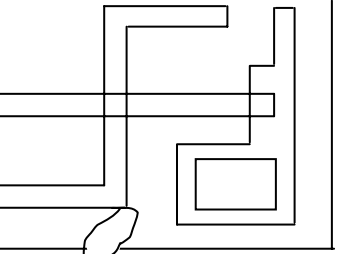
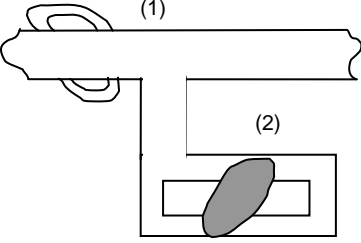
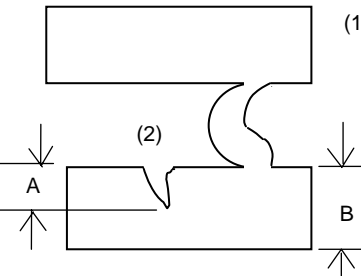
Wafer thickness: 350 μm

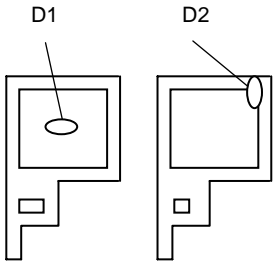
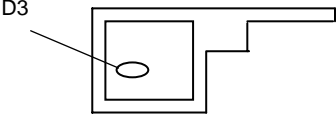
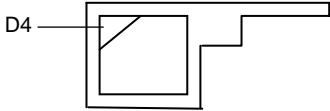
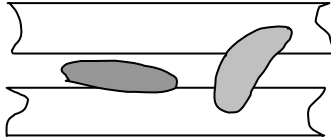
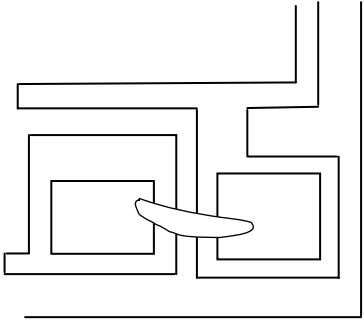
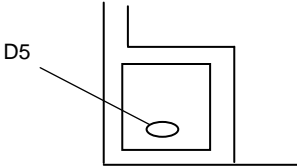
Scribe Line Layout Diagram (unit: micron)



Sensor dimension: 90 μm x 60 μm

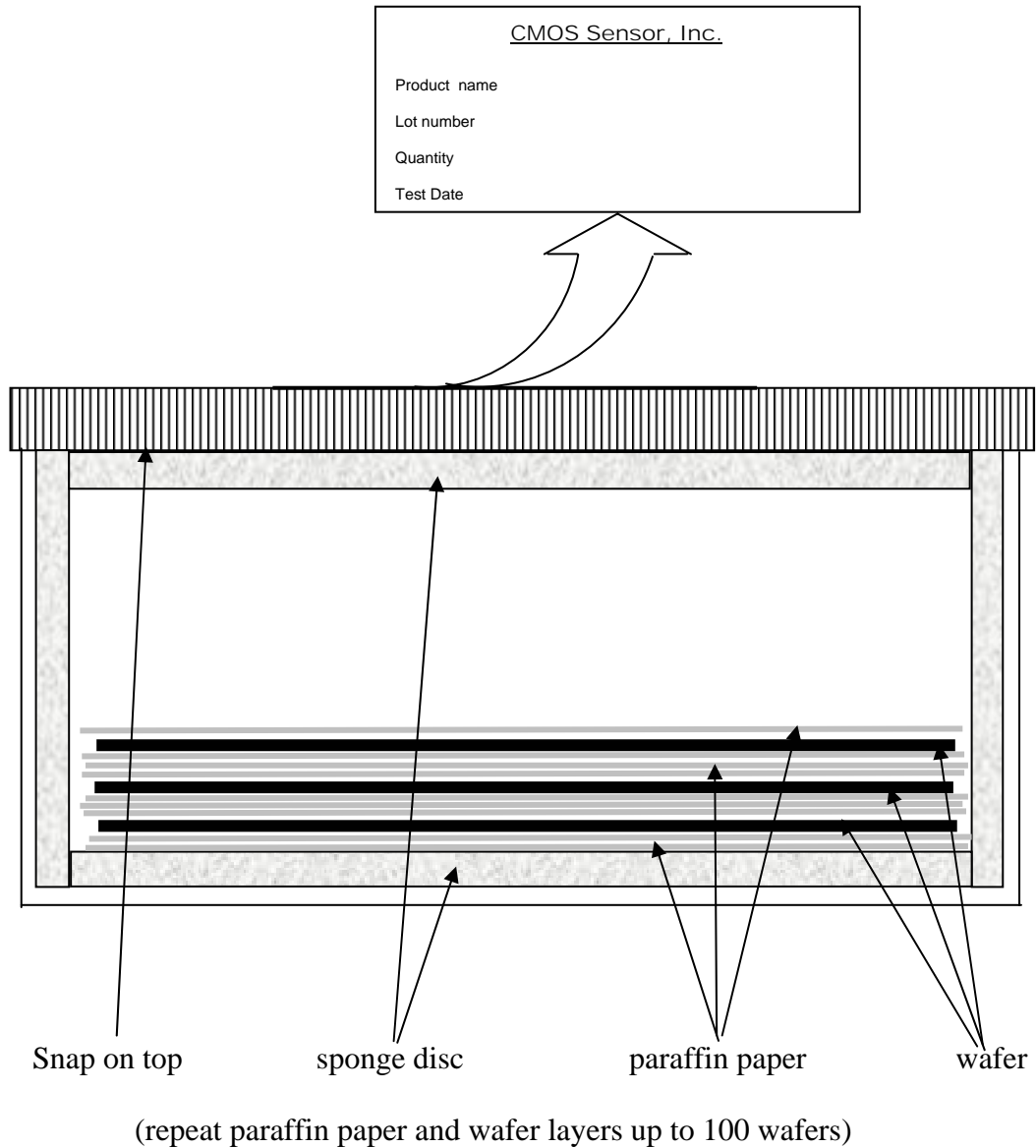
Microscope Inspection Specifications

No.	ITEMS	INSPECTION CRITERION	SIMPLIFIED DIAGRAM
1	BAD METAL LINE	(1) DEFICIENT AND VOID METAL LINE $A \geq B/2$	
		(2) PROXIMITY AND SHORTING OF METAL LINE $A \leq B/2$ C IS SHORTED	
		(3) HILLOCK	
		(4) METAL RESIDUES	
2	BAD OXIDE LAYER	(1) OXIDE LAYER VOID UNDER METAL LINE	
		(2) OXIDE LAYER VOID ON METAL LINE TO THE ACTIVE DEVICE	
3	BAD DIFFUSION	(1) SHORT BETWEEN TWO DIFFUSION REIGONS	
		(2) DEFICIT DIFFUSION REGION $A \geq B/2$	

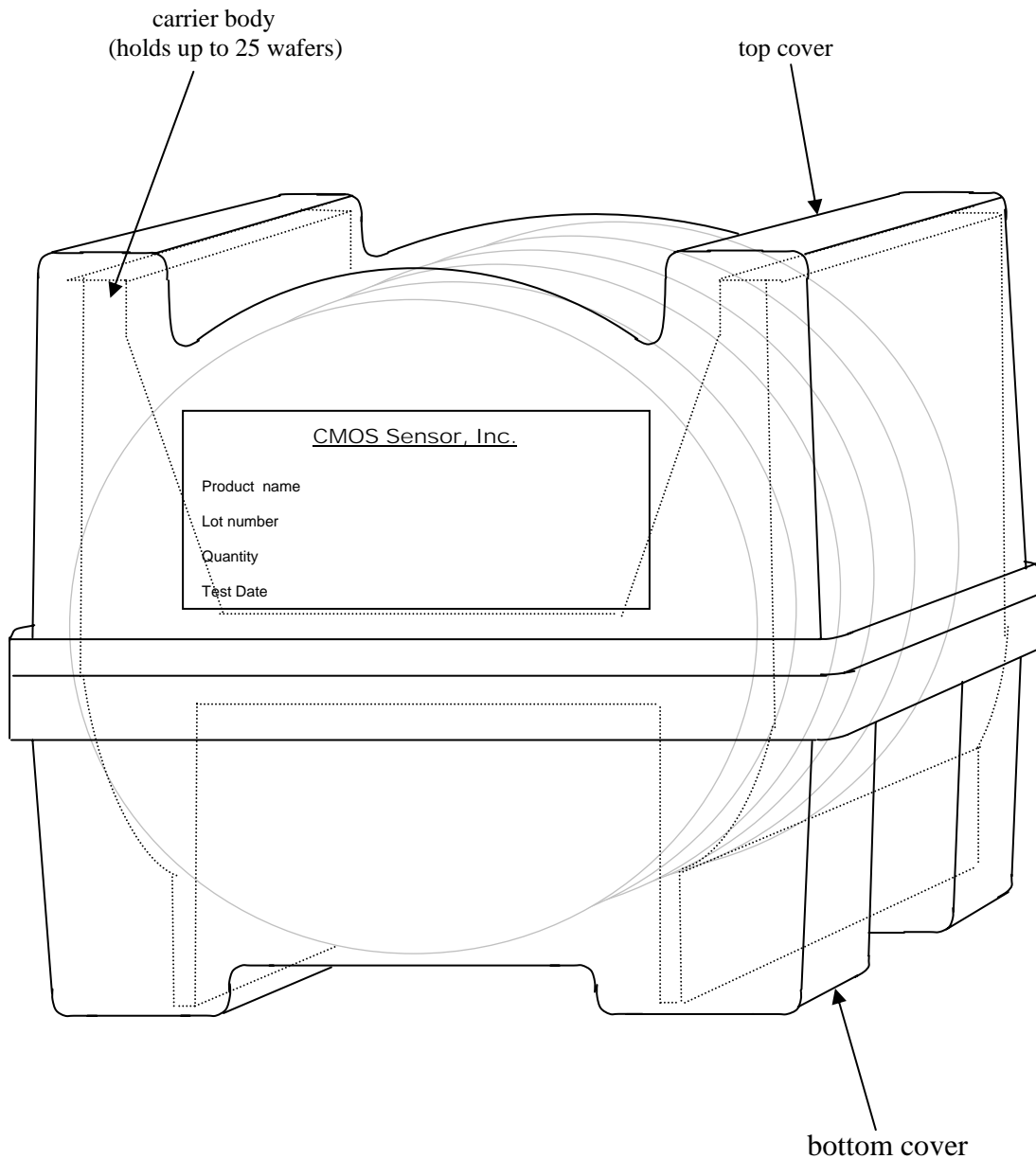
No.	ITEMS	INSPECTION CRITERION	SIMPLIFIED DIAGRAM
4	BAD BONDING PAD	(1) METAL LAYER VOID EITHER WITHIN PAD OR AT CORNER $D1 \geq D/5$ $D2 \geq D/5$ WHERE D IS THE SIZE OF THE BONDING PAD	
		(2) DISCOLORIZATION OF THE BONDING PAD METAL $D3 \geq D/5$	
		(3) MISSING BONDING PAD METAL	
5	BAD PASSIVATION LAYER	(1) PASSIVATION RESIDUE WITHIN PAD $D4 \geq D/5$ WHERE D IS THE PAD SIZE	
		(2) PASSIVATION VOID ON METAL LINES OR BE- TWEEN METAL LINES	
6	CONTAMINATION AND FOREIGN PARTICLES	(1) CONTAMINATION OR FOREIGN PARTICLE (a) WHICH HAS A SIZE GREATER THAN 50 MICRONS (b) WHICH CONNECTS BETWEEN TWO EXPOSED METAL PATTERNS	
		(2) CONTAMINATION OR FOREIGN PARTICLE ON THE BONDING PAD $D5 \geq D/5$	

Shipping Package

1. Basically, wafers in the containers shown are manufactured under the same conditions at the same time.
2. Wafers may be shipped in either of two package types:
 - (1) a round shipping package.
 - (2) a molded wafer shipper.



(1) ROUND SHIPPING PACKAGE



(2) MOLDED WAFER SHIPPER

3. Identification

A label should be attached to each shipping container.
The label must include the following items:

- (1) product name
- (2) lot number
- (3) quantity
- (4) test date

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