

7400 PIXELS CCD LINEAR IMAGE SENSOR

The μ PD3747 is a high-speed and high sensitive CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μ PD3747 is a 2-output type CCD sensor with 2 rows of high-speed charge transfer register, which transfers the photo signal electrons of 7400 pixels separately in odd and even pixels. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 600 dpi/A3 high-speed digital copiers, multi-function products and so on.

FEATURES

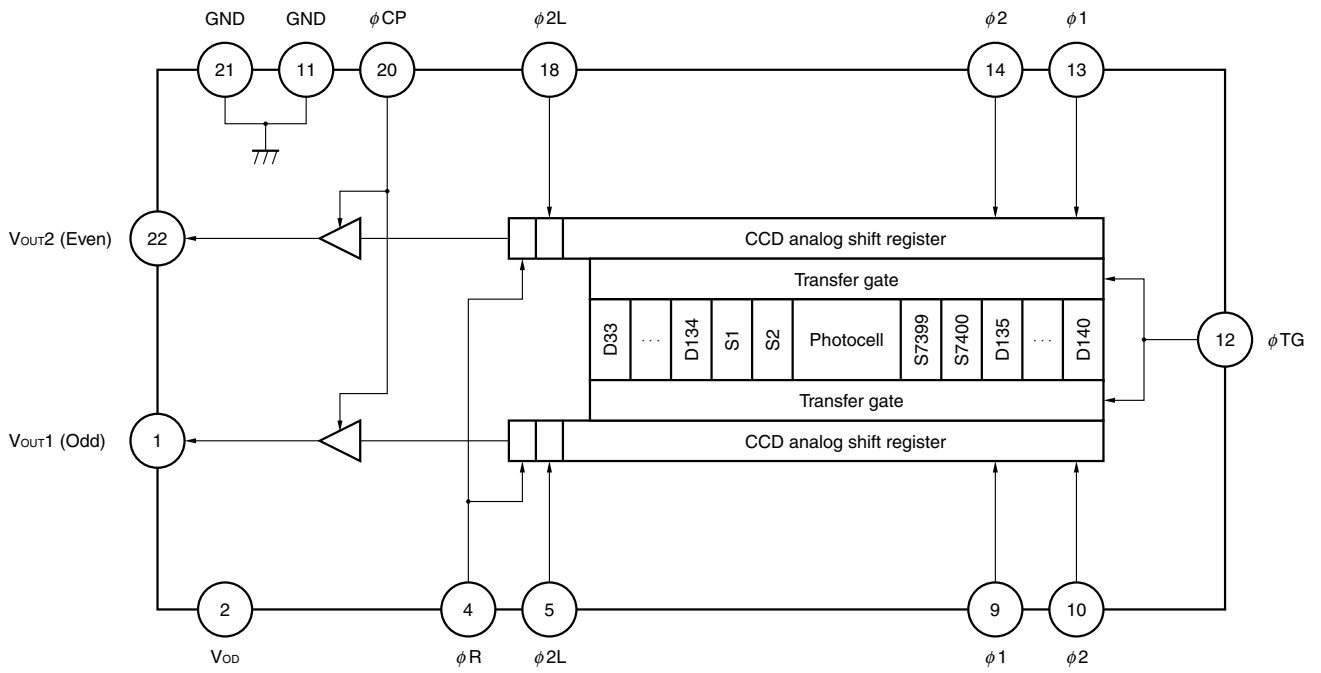
- Valid photocell : 7400 pixels
- Photocell pitch : 4.7 μ m
- Photocell size : 4.7 \times 4.7 μ m²
- Resolution : 24 dot/mm (600 dpi) A3 (297 \times 420 mm) size (shorter side)
- Data rate : 44 MHz MAX. (22 MHz/1 output)
- Output type : 2 outputs in phase
- High sensitivity : 19.0 V/lx \cdot s TYP. (Light source: Daylight color fluorescent lamp)
- Low image lag : 1 % MAX.
- Power supply : +12 V
- Drive clock level : CMOS output under 5 V operation
- On-chip circuits : Reset feed-through level clamp circuits
Voltage amplifiers

ORDERING INFORMATION

| Part Number | Package |
|---------------|--|
| μ PD3747D | CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400)) |

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

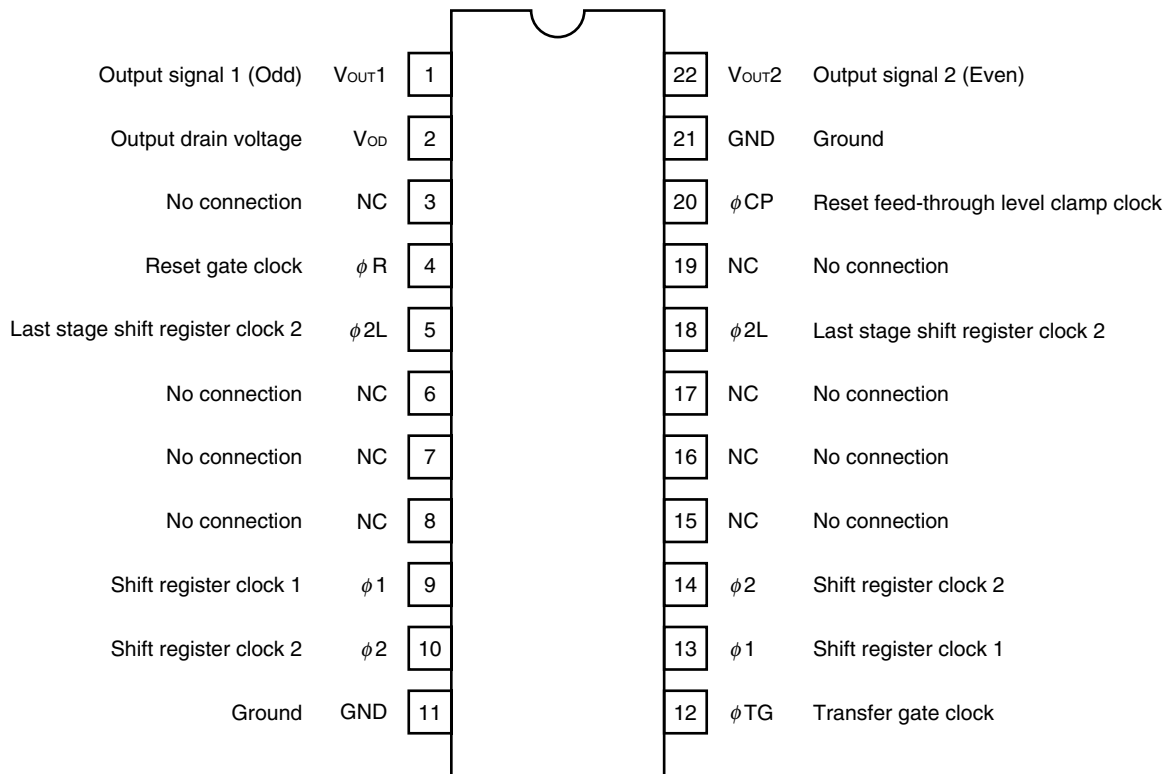
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

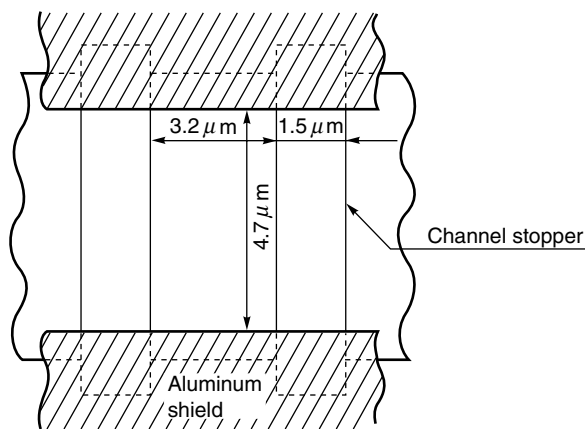
CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

• μPD3747D



Caution Connect the No connection pins (NC) to GND.

PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

| Parameter | Symbol | Ratings | Unit |
|---|--|-------------|------|
| Output drain voltage | V _{OD} | -0.3 to +14 | V |
| Shift register clock voltage | V _{φ1} , V _{φ2} , V _{φ2L} | -0.3 to +8 | V |
| Reset gate clock voltage | V _{φR} | -0.3 to +8 | V |
| Reset feed-through level clamp clock voltage | V _{φCP} | -0.3 to +8 | V |
| Transfer gate clock voltage | V _{φTG} | -0.3 to +8 | V |
| Operating ambient temperature ^{Note} | T _A | -25 to +55 | °C |
| Storage temperature | T _{stg} | -40 to +100 | °C |

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|------|------|------|------|
| Output drain voltage | V _{OD} | 11.4 | 12.0 | 12.6 | V |
| Shift register clock high level | V _{φ1H} , V _{φ2H} , V _{φ2LH} | 4.5 | 5.0 | 5.5 | V |
| Shift register clock low level | V _{φ1L} , V _{φ2L} , V _{φ2LL} | -0.3 | 0 | +0.5 | V |
| Reset gate clock high level | V _{φRH} | 4.5 | 5.0 | 5.5 | V |
| Reset gate clock low level | V _{φRL} | -0.3 | 0 | +0.5 | V |
| Reset feed-through level clamp clock high level | V _{φCPH} | 4.5 | 5.0 | 5.5 | V |
| Reset feed-through level clamp clock low level | V _{φCPL} | -0.3 | 0 | +0.5 | V |
| Transfer gate clock high level | V _{φTGH} | 4.5 | 5.0 | 5.5 | V |
| Transfer gate clock low level | V _{φTGL} | -0.3 | 0 | +0.5 | V |
| Data rate | 2f _{φR} | 1 | 2 | 44 | MHz |

ELECTRICAL CHARACTERISTICS

($T_A = +25^{\circ}\text{C}$, $V_{OD} = 12\text{ V}$, $f_{\phi R} = 1\text{ MHz}$, data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V_{p-p},
light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm))

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------------|--|------|------|------|--------|
| Saturation voltage | V _{sat} | | 1.5 | 2.0 | – | V |
| Saturation exposure | SE | Daylight color fluorescent lamp | – | 0.10 | – | lx•s |
| Photo response non-uniformity | PRNU | V _{OUT} = 500 mV | – | 5 | 10 | % |
| Average dark signal | ADS | Light shielding | – | 0.5 | 3.0 | mV |
| Dark signal non-uniformity | DSNU | Light shielding | – | 8.0 | 14.0 | mV |
| Power consumption | P _w | | – | 350 | 600 | mW |
| Output impedance | Z _o | | – | 0.2 | 0.3 | kΩ |
| Response | R _F | Daylight color fluorescent lamp | 13.3 | 19.0 | 24.7 | V/lx•s |
| Image lag | IL | V _{OUT} = 500 mV | – | 0.5 | 1.0 | % |
| Offset level ^{Note 1} | V _{OS} | | 3.7 | 4.7 | 5.7 | V |
| Output fall delay time ^{Note 2} | t _d | V _{OUT} = 500 mV | – | 14 | – | ns |
| Register imbalance | RI | V _{OUT} = 500 mV | 0 | 1.0 | 4.0 | % |
| Total transfer efficiency | TTE | V _{OUT} = 1 V, data rate = 44 MHz | 94 | 98 | – | % |
| Response peak | | | – | 550 | – | nm |
| Dynamic range | DR1 | V _{sat} /DSNU | – | 250 | – | times |
| | DR2 | V _{sat} /σ bit | – | 1000 | – | times |
| Reset feed-through noise ^{Note 1} | RFTN | Light shielding | –300 | +300 | +900 | mV |
| Random noise | σ bit | Light shielding, bit clamp mode | – | 2.0 | – | mV |
| | σ line | Light shielding, line clamp mode | – | 8.0 | – | mV |
| Shot noise | σ shot | V _{OUT} = 500 mV, bit clamp mode | – | 8.0 | – | mV |

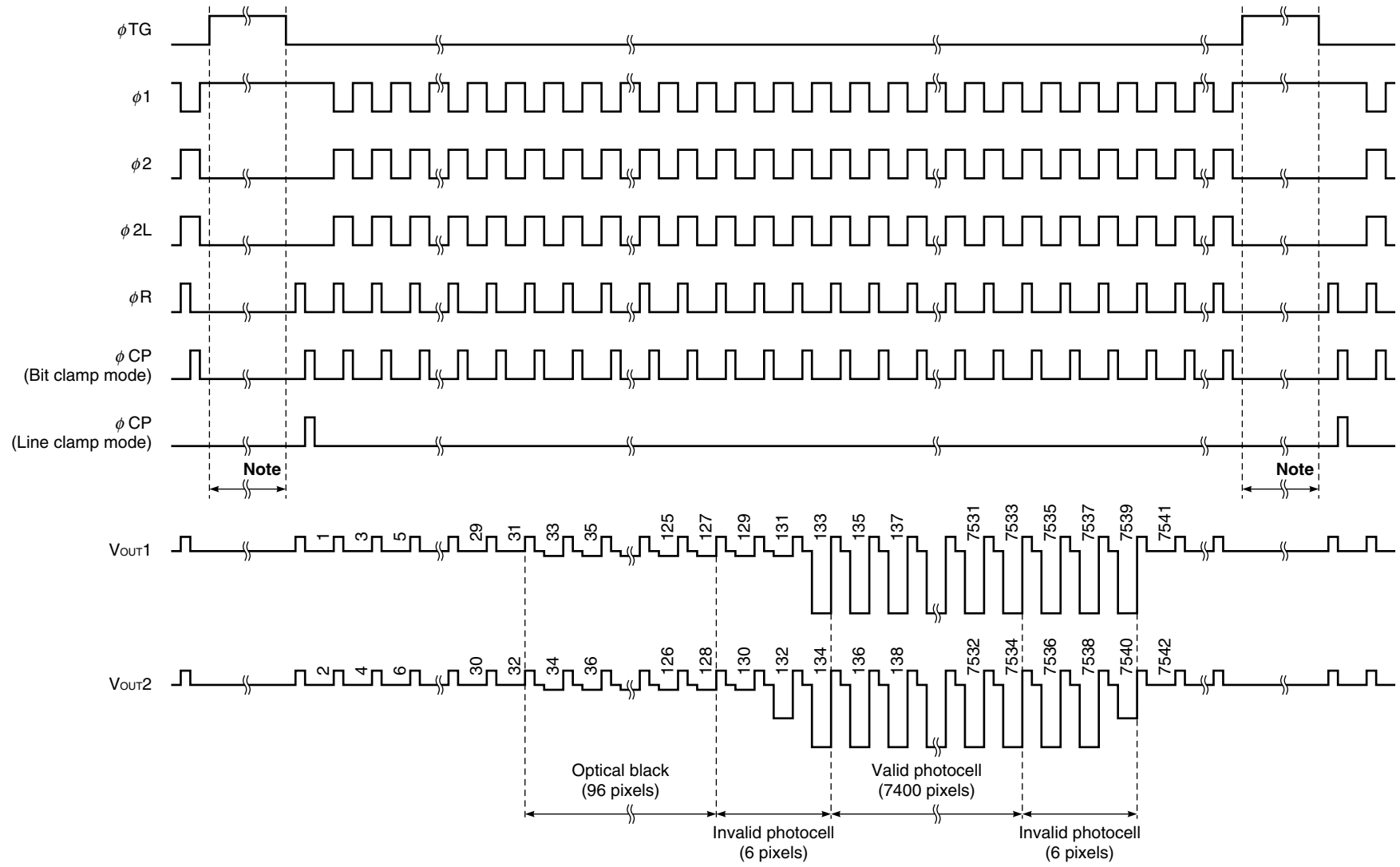
Notes 1. Refer to **TIMING CHART 2, 3.**

2. When the fall time of φ 2L (t₂¹) is the TYP. value (refer to **TIMING CHART 2, 3**). Note that V_{OUT1} and V_{OUT2} are the outputs of the two steps of emitter-follower shown in **APPLICATION CIRCUIT EXAMPLE**.

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

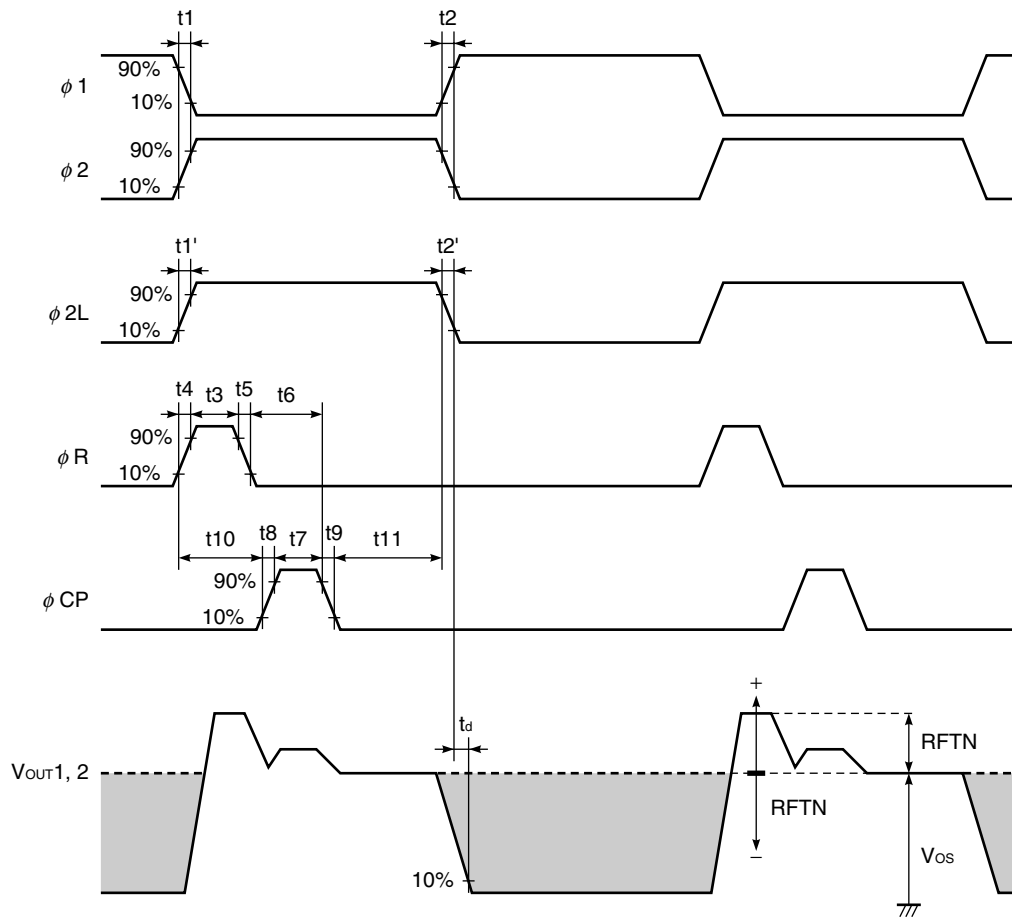
| Parameter | Symbol | Pin name | Pin No. | MIN. | TYP. | MAX. | Unit |
|--|------------------|----------|---------|------|------|------|------|
| Shift register clock pin capacitance 1 | C _{φ1} | φ 1 | 9 | – | 250 | 300 | pF |
| | | | 13 | – | 250 | 300 | pF |
| Shift register clock pin capacitance 2 | C _{φ2} | φ 2 | 10 | – | 250 | 300 | pF |
| | | | 14 | – | 250 | 300 | pF |
| Last stage shift register clock pin capacitance | C _{φL} | φ 2L | 5 | – | 10 | 20 | pF |
| | | | 18 | – | 10 | 20 | pF |
| Reset gate clock pin capacitance | C _{φR} | φ R | 4 | – | 10 | 20 | pF |
| Reset feed-through level clamp clock pin capacitance | C _{φCP} | φ CP | 20 | – | 10 | 20 | pF |
| ★ Transfer gate clock pin capacitance | C _{φTG} | φ TG | 12 | – | 250 | 300 | pF |

TIMING CHART 1



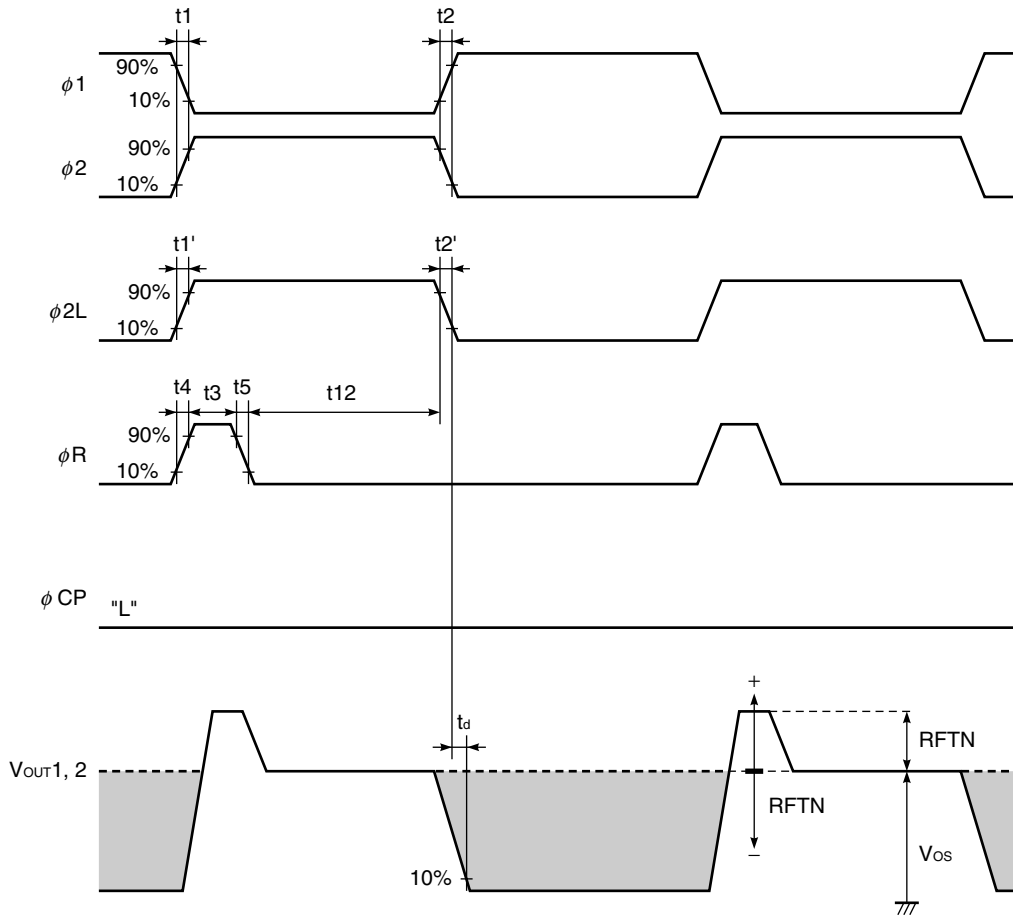
Note Set the ϕR and ϕCP to low level during this period.

TIMING CHART 2 (Bit clamp mode)



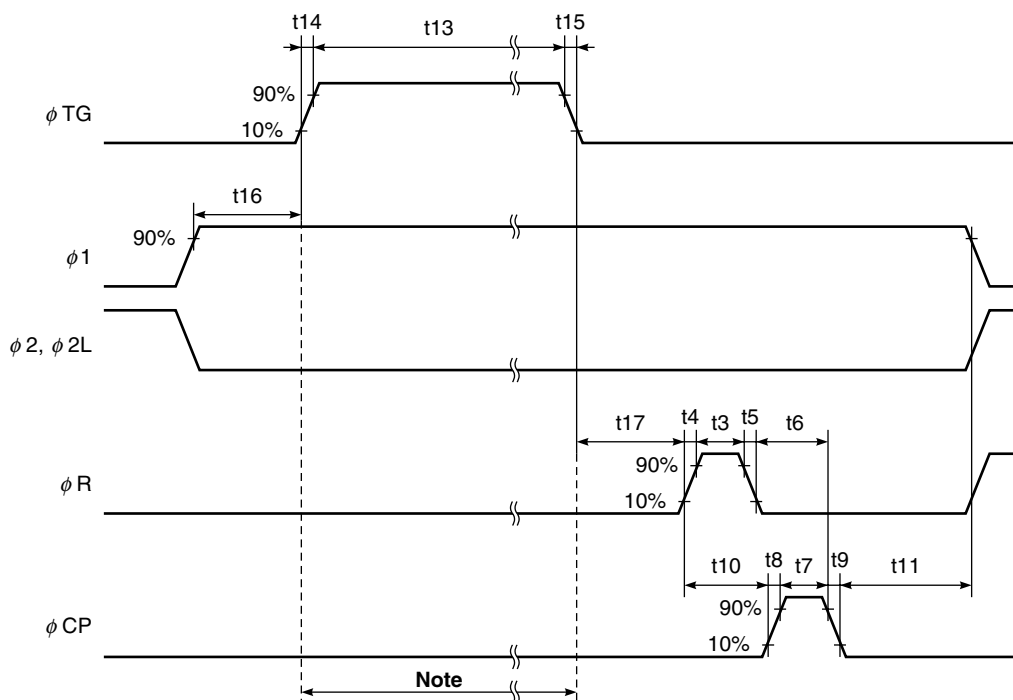
| Symbol | MIN. | TYP. | MAX. | Unit |
|------------|------|------|------|------|
| $t1, t2$ | 0 | 50 | – | ns |
| $t1', t2'$ | 0 | 5 | – | ns |
| $t3$ | 10 | 125 | – | ns |
| $t4, t5$ | 0 | 5 | – | ns |
| $t6$ | 0 | 125 | – | ns |
| $t7$ | 5 | 125 | – | ns |
| $t8, t9$ | 0 | 5 | – | ns |
| $t10$ | $t3$ | 125 | – | ns |
| $t11$ | 0 | 250 | – | ns |

TIMING CHART 3 (Line clamp mode)



| Symbol | MIN. | TYP. | MAX. | Unit |
|------------|------|------|------|------|
| $t1, t2$ | 0 | 50 | – | ns |
| $t1', t2'$ | 0 | 5 | – | ns |
| $t3$ | 10 | 125 | – | ns |
| $t4, t5$ | 0 | 5 | – | ns |
| $t12$ | 5 | 250 | – | ns |

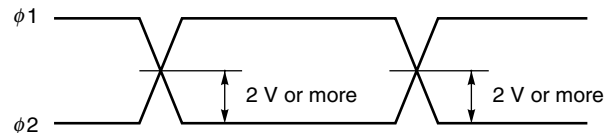
TIMING CHART 4 (Bit clamp mode, Line clamp mode)



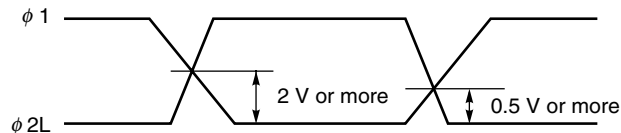
Note Set the ϕ R and ϕ CP to low level during this period.

| Symbol | MIN. | TYP. | MAX. | Unit |
|----------|------|------|------|------|
| t3 | 10 | 125 | – | ns |
| t4, t5 | 0 | 5 | – | ns |
| t6 | 0 | 125 | – | ns |
| t7 | 5 | 125 | – | ns |
| t8, t9 | 0 | 5 | – | ns |
| t10 | t3 | 125 | – | ns |
| t11 | 0 | 250 | – | ns |
| t13 | 1000 | 1500 | – | ns |
| t14, t15 | 0 | 50 | – | ns |
| t16, t17 | 200 | 300 | – | ns |

ϕ 1, ϕ 2 cross points



ϕ 1, ϕ 2L cross points



Remark Adjust cross points of (ϕ 1, ϕ 2) and (ϕ 1, ϕ 2L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

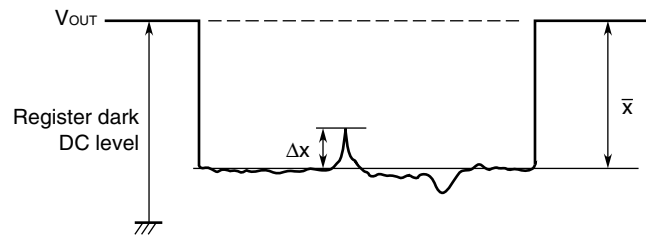
1. Saturation voltage : **V_{sat}**
Output signal voltage at which the response linearity is lost.
2. Saturation exposure : **SE**
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.
3. Photo response non-uniformity : **PRNU**
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

Δx: maximum of $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{7400} x_j}{7400}$$

x_j: Output voltage of valid pixel number j



4. Average dark signal : **ADS**
Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS (mV) = \frac{\sum_{j=1}^{7400} d_j}{7400}$$

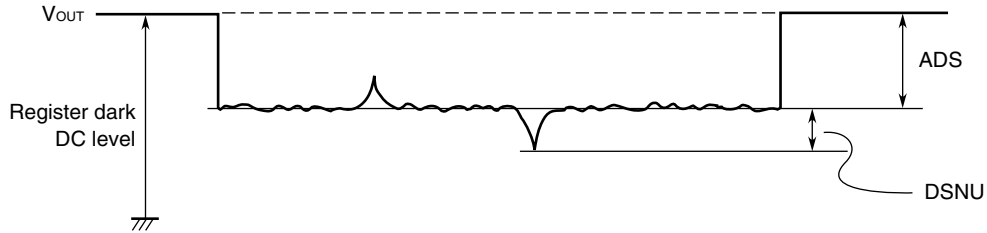
d_j: Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV): maximum of $|d_j - ADS|$ $|_{j = 1 \text{ to } 7400}$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

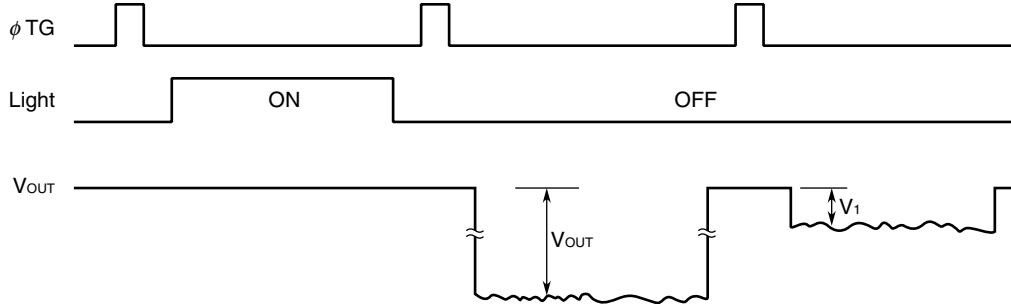
7. Response : **R**

Output voltage divided by exposure ($lx \cdot s$).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.

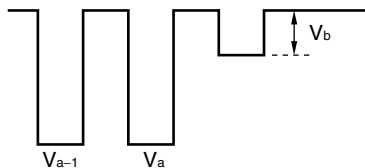


$$IL (\%) = \frac{V_1}{V_{OUT}} \times 100$$

★ 9. Total transfer efficiency : **TTE**

The total transfer rate of CCD analog shift register. This is calculated by the following formula, it is defined by each output.

$$TTE (\%) = (1 - V_b / \text{average output of all the valid pixels}) \times 100$$



V_{a-1} : The last pixel output - 1 (Odd pixel: 7537th pixel)

V_a : The last pixel output (Odd pixel: 7539th pixel)

V_b : The split pixel output (Odd pixel: 7541st pixel)

10. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

n : Number of valid pixels

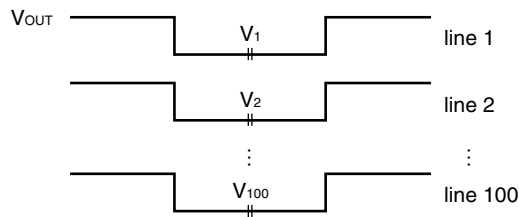
V_j: Output voltage of each pixel

11. Random noise : **σ**

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

$$\sigma (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

V_i: A valid pixel output signal among all of the valid pixels



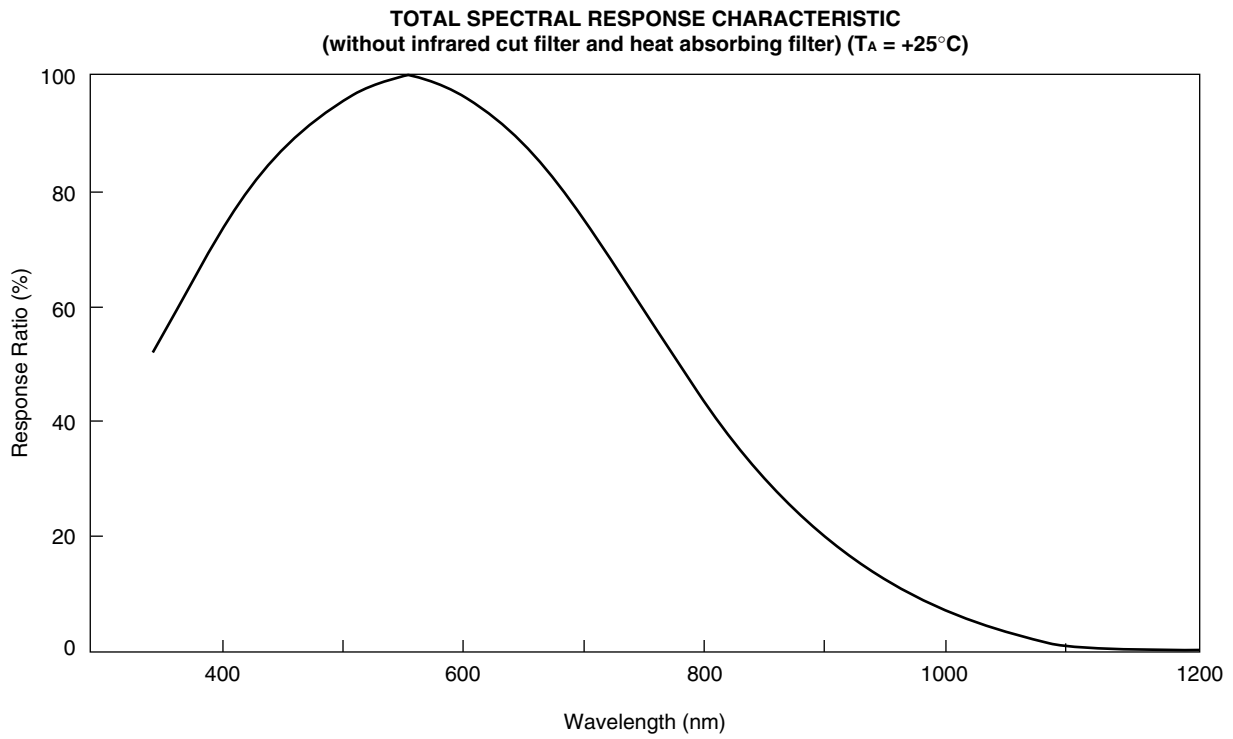
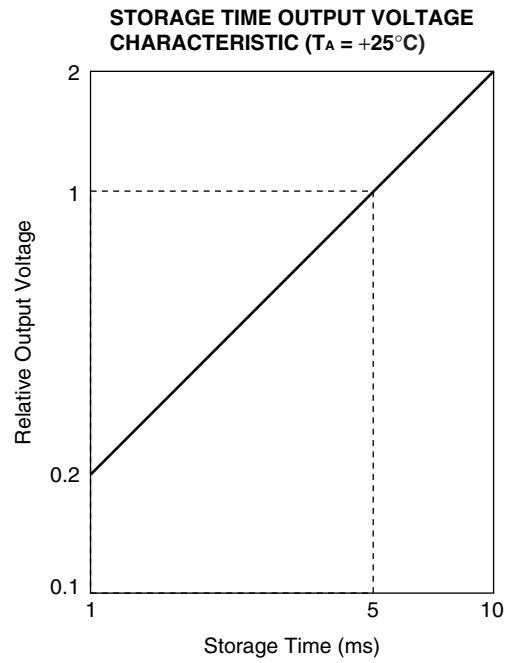
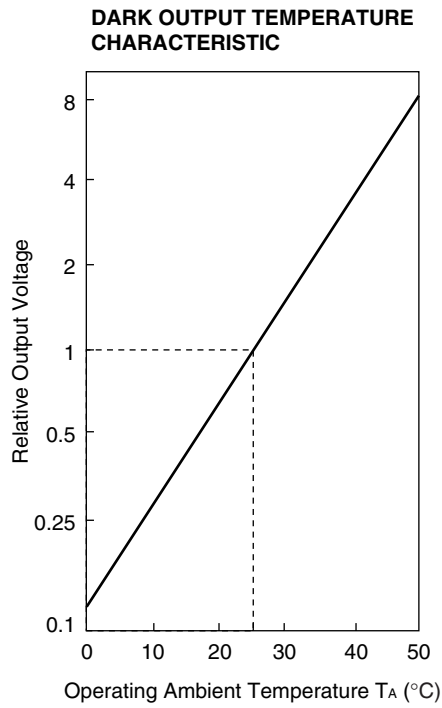
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

12. Shot noise : **σ_{shot}**

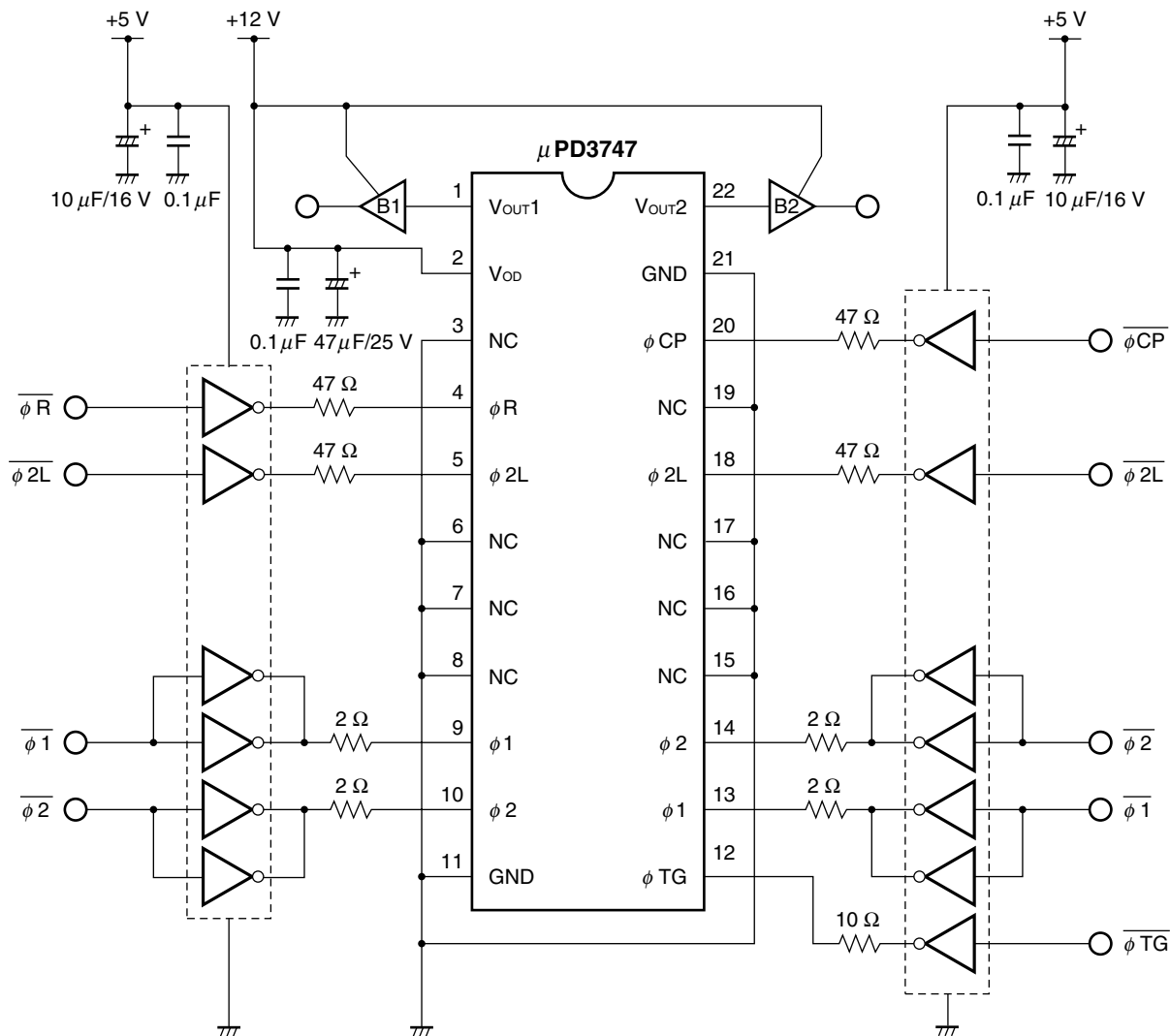
Shot noise is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling in the light. This includes the random noise.

The formula is the same with that of random noise.

STANDARD CHARACTERISTIC CURVES (Reference Value)



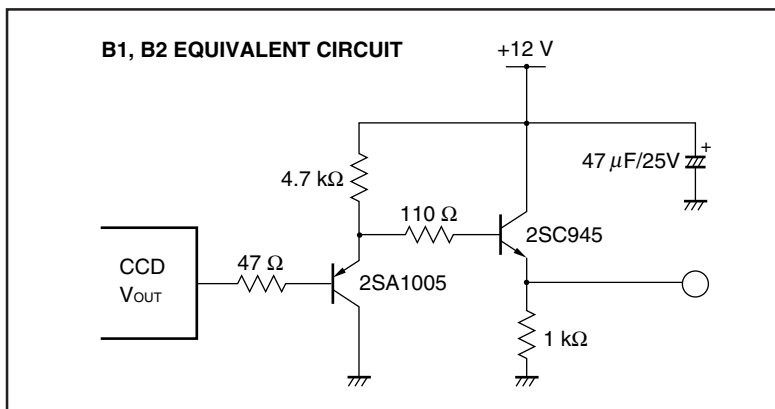
APPLICATION CIRCUIT EXAMPLE



Caution Connect the No connection pins (NC) to GND.

Remarks 1. It is recommended that pins 5 and 18 (φ 2L) are separately driven a driver other than that of pins 10, 14 (φ 2).

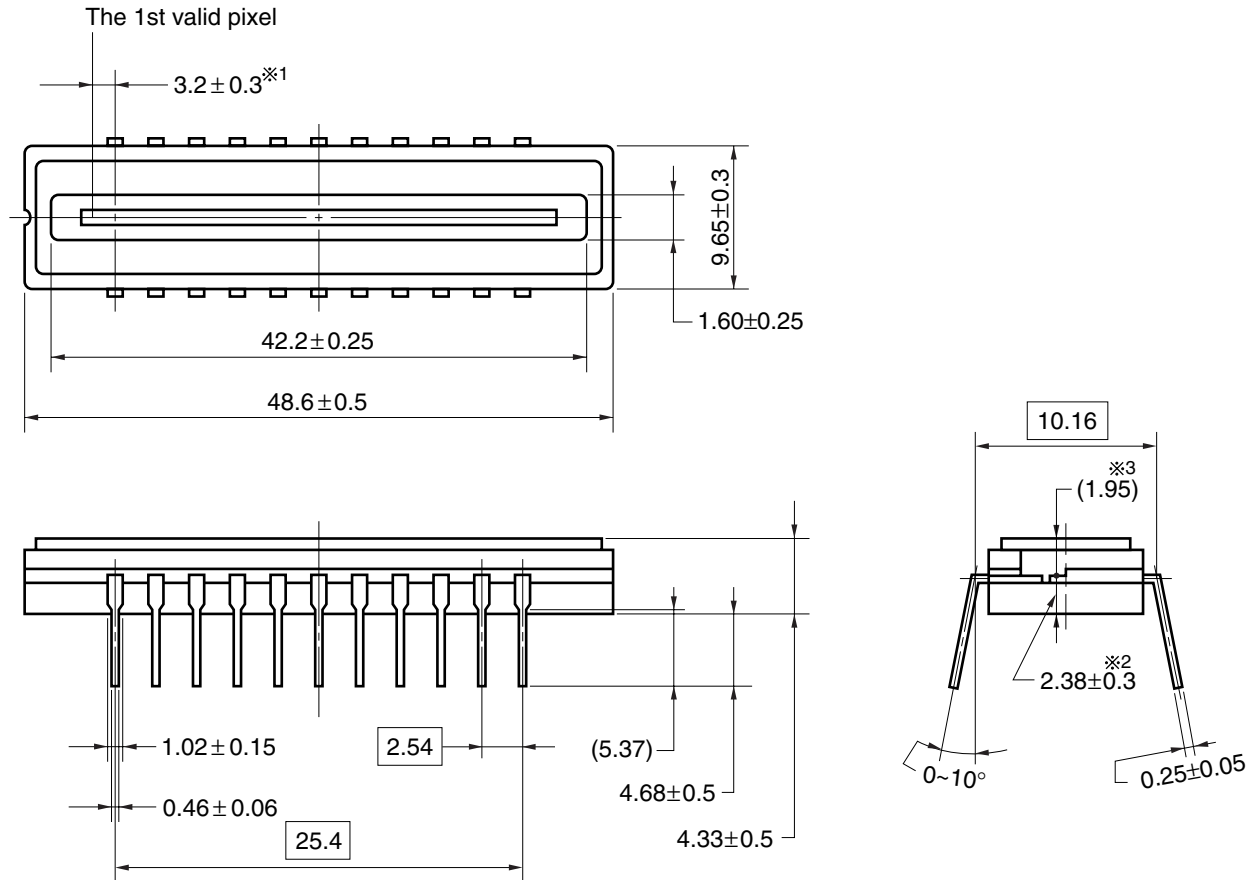
2. The inverters shown in the above application circuit example are the 74AC04.



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 22-PIN CERAMIC DIP (CERDIP) (10.16 mm (400))

(Unit : mm)



| Name | Dimensions | Refractive index |
|-----------|---------------|------------------|
| Glass cap | 47.5×9.25×0.7 | 1.5 |

- ※ 1 1st valid pixel ↔ Center of pin 1
- ※ 2 Photosensitive surface of CCD chip ↔ Bottom of package
- ※ 3 Photosensitive surface of CCD chip ↔ Top of glass cap

22D-1CCD-PKG10

★ **RECOMMENDED SOLDERING CONDITIONS**

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD3747D : CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

| Process | Conditions |
|------------------------|---|
| Partial heating method | Pin temperature : 300°C or below, Heat time : 3 seconds or less (per pin) |

- Cautions**
1. **During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.**
 2. **Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.**

★

NOTES ON HANDLING THE PACKAGES

① MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with glass cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

② GLASS CAP

Don't either touch glass cap surface by hand or have any object come in contact with glass cap surface. Care should be taken to avoid mechanical or thermal shock because the glass cap is easily to damage. For dirt stuck through electricity ionized air is recommended.

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers or of pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information in this document is current as of September, 2002. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
 - No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
 - NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
 - Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
 - While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
 - NEC semiconductor products are classified into the following three quality grades:
"Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
"Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
"Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
"Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
- The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
- (Note)
- (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
 - (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).